HX9035

Features

- **1.8V Single Supply**
- **five sensor inputs**
- **Capacitance resolution up to 0.59aF**
- **Capacitance offset compensation up to 800pF**
- **Support fully differential input mode**
- **Smart SAR detection engine**
- **Advanced ambient environment compensation algorithm**
- **Automatic adaptive threshold and sensitivity levels**
- **Programmable detection range**
- **Programmable scan period from 2ms to 4s**
- **Ultra-low EMI mode by enable spread spectrum**
- **Integrated temperature sense ADC for temperature compensation**
- **Three level user proximity interrupts**
- **Low Power consumption**
  Scan Mode: 25 uA
  Doze Mode: 7 uA
  Sleep Mode: 3 uA
- **Support up to 400kHz I2C Serial Interface**
- **Support 1.2V~3.6V IO voltage**
- **Programmable Interrupt or Real-Time Status Pin**
- **-40°C to +85°C Operation**
- **Compact Size: 1.17mm x 1.24mm WLCSP9 package**

Applications

Smart Phone, PAD, TWS
Head Phone, Smart Wearable

Description

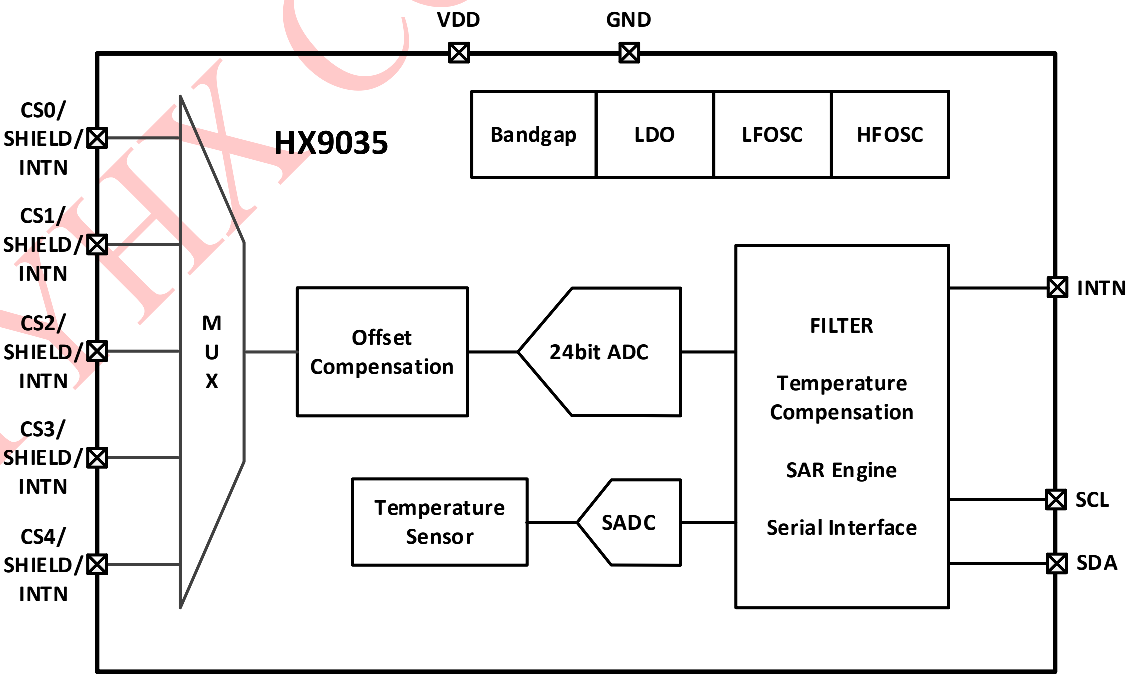
The HX9035 integrates a capacitance sense AFE used for Specific Absorption Rate (SAR) application.

The HX9035 supports up to five sensor inputs, with an offset compensation capacitance up to 800pF. The HX9035 has high sensitivity which enables the detection of human body proximity. The portable electronic device can reduce the emission power upon the presence of human body according to the detection result of HX9035. This will bring significant performance advantages for manufacturers of electronic devices with electro-magnetic radiation sources to meet stringent emission regulations' criteria and Specific Absorption Rate (SAR) standards.

The HX9035 can operate from 1.8V single supply, and it outputs data via I2C bus. The I2C serial communication bus port is compatible with 1.2V~3.6V host control to report user proximity. Upon proximity detection, the INTN output asserts, enabling the user to either determine the relative proximity distance, or simply obtain an indication of detection.

HX9035 has on-chip calibration logic to account for changes in the ambient environment, such as temperature, humidity. The calibration sequence is performed automatically and at continuous intervals, while the sensors are not touched. This ensures that there are no false detections on the external sensors due to the changing environment

Simplified Block Diagram



Contents

1 Pin Configuration

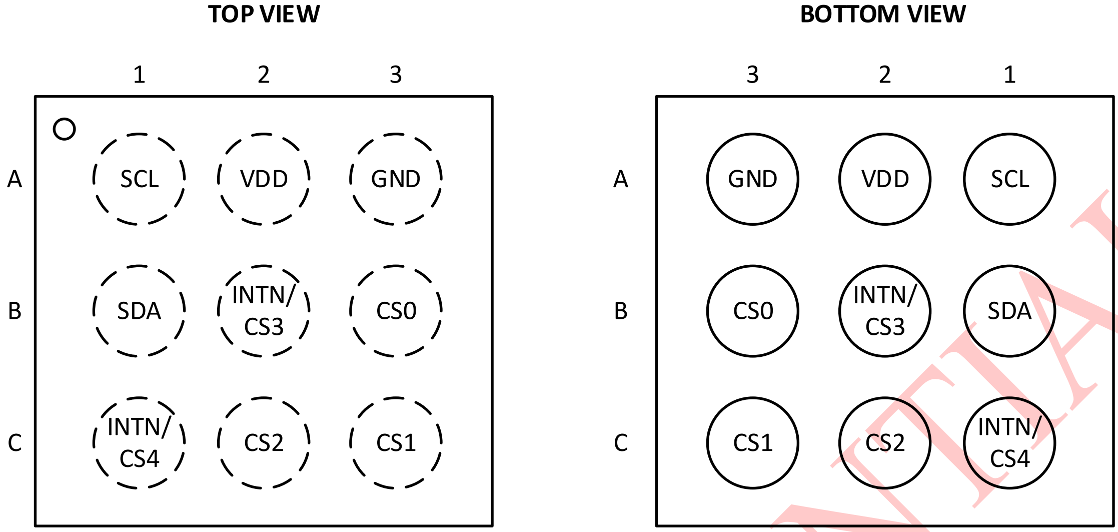


Figure1 HX9035 Pin Diagram

Table1 HX9035 Pin Description

Pin	Name	Type	Description
A1	SCL	Digital	I2C CLK, external pull up resistor (recommended 2.2kΩ for 400KHz)
A2	VDD	Power	Power Supply
A3	GND	Ground	Power Ground
B1	SDA	Digital	I2C data, external pull up resistor (recommended 2.2kΩ for 400KHz)
B2	INTN/CS3	Analog	Interrupt/Capacitance Sensor Input.
B3	CS0/INTN	Analog	Capacitance Sensor Input/Interrupt.
C1	INTN/CS4	Analog	Interrupt/Capacitance Sensor Input.
C2	CS2/INTN	Analog	Capacitance Sensor Input/Interrupt.
C3	CS1/INTN	Analog	Capacitance Sensor Input/Interrupt.

2 Specifications

2.1 Absolute Maximum Rating

Parameter	Symbol	Min	Max	Unit
Supply Voltage	VDD	-0.5	2	V
Pull-up Voltage	VPULL	-0.5	3.6	V
Input Voltage(non-supply pins)	VIN	-0.5	VDD+0.3	V
Input Current(non-supply pins)	IIN	-10	10	mA
Operating Junction Temperature	TJCT	-40	125	℃
Reflow Temperature	TRE		260	℃
Storage Temperature	TSTOR	-50	150	℃

2.1 Recommended Operating Conditions

Parameter	Min	Max	Unit
VDD	1.65	1.98	V
Specified temperature range	-40	85	℃

2.3 ESD Ratings

Parameter		Value	Unit
V(ESD) Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	±2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101	±500	

2.4 Electrical Characteristics

Typical specifications are at 25°C, VDD 1.8V, offset capacitor 30pF, OSR = 128, ODR = 5Hz, minimum and maximum specifications are at VDD = 1.62V to 1.98 V, Temp = −40°C to +85°C, unless otherwise noted.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Conversion Rate	2	200	4000	ms	Programmable
Resolution	1		100	aF/LSB	Programmable
Input Range	±1.25		±10	pF	Programmable
Input Channel Linearity		±3		fF	
Sampling Frequency	4		800	kHz	
RMS Noise @30pF load		15		aF	
RMS Noise @200pF load		100		aF	
Input Leakage			1	nA	
Gain Error			3	%	
Offset Compensation Range			800	pF	
Offset Compensation Resolution		26		fF	
Input RC Resistor	400		4k	Ω	Programmable
Input RC Capacitor		5		pF	
Total Internal Channel Capacitance		6		pF	Total channel capacitance measured at the ball; guaranteed by design
Current Consumption					
Full Power		1.2		mA	1KHz conversation rate
Scan Mode		25		µA	OSR=128, Single channel, ODR=5Hz
Doze Mode		7		µA	OSR=128, Single channel, ODR=2.5Hz
Sleep Mode		3		uA	Sleep Mode
Inputs SCL,SDA					
Input High Voltage, VIH	0.7 × VIO			V	
Input Low Voltage, VIL			0.2 × VDD	V	
Input High Current, IIH	−1			µA	VIN = 1.8
Input Low Current, IIL			1	µA	VIN = 0V
Open-Drain Outputs (SDA, INTN)					

Output Low Voltage, VOL			+0.3 × VIO	V	ISINK = −3 mA
Output High Leakage Current, IOH		±0.1	±1	µA	VOUT = 1.8 V
INTERNAL OSCILLATOR					
HFOSC Frequency		5		MHz	
HFOSC Accuracy			±4	%	
LFOSC Frequency		32		kHz	
LFOSC Accuracy			±4	%	
POWER-ON RESET					
Power-Down Level			0.2	V	−40°C to +85°C, VDD = 1.8 V
Power-On Level	1.5			V	−40°C to +85°C, VDD = 1.8 V
VDD	1.65		1.98	V	

3 Detailed Description

3.1 Overview

The HX9035 integrates a capacitance sense AFE used for Specific Absorption Rate (SAR) application. The HX9035 supports up to five sensor inputs, with an offset compensation capacitance up to 800pF. The HX9035 has high sensitivity which enables the detection of human body proximity. The portable electronic device can reduce the emission power upon the presence of human body according to the detection result of HX9035. This will bring significant performance advantages for manufacturers of electronic devices with electro-magnetic radiation sources to meet stringent emission regulations' criteria and Specific Absorption Rate (SAR) standards.

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3.2 Functional Block Diagram

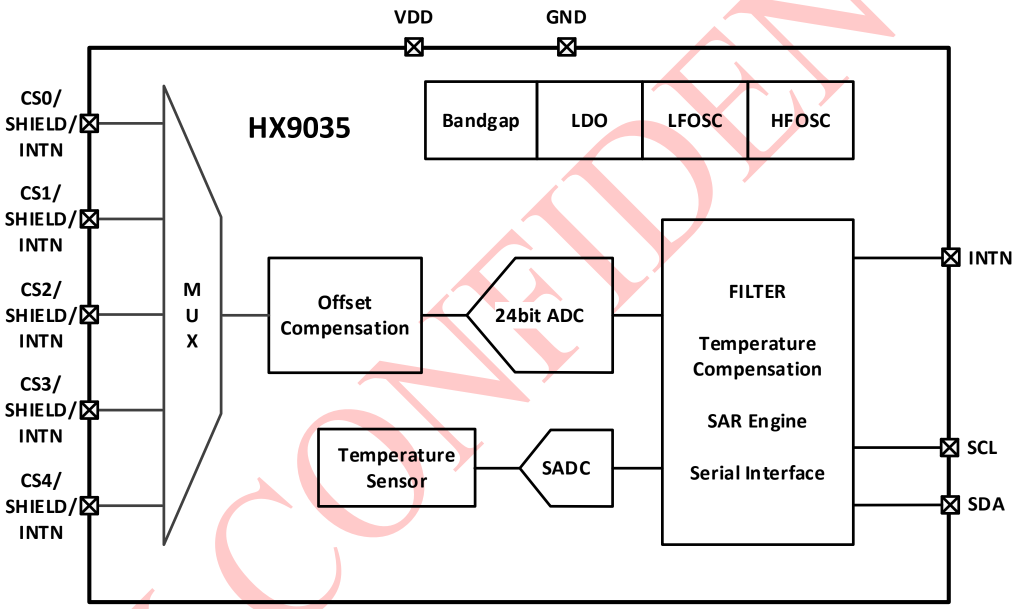


Figure2 Functional Block Diagram

3.3 Working Mode

HX9035 has mainly three operation modes

1 sleep mode: which is configured if no CH_EN is enabled. All the circuits except I2C and 32KHz OSC are shut down and the power consumption is less than 4uA.

2 scan mode: if any of the CH_NUM[4:0] is enabled, HX9035 will go to scan mode, in this mode the chip will periodically detect the capacitance on each sensor (if enabled). The scan period can be configured by register.

3 doze mode: In some applications, the reaction/sensing time needs to be fast when the user is present (proximity detected), but can be slow when no detection has occurred for some time. If DOZE_EN is enabled, the HX9035 will scan each channel (if enabled) by a relatively slow rate, and if user proximity is detected, it will accelerate the scan period and back to slow rate when proximity is released.

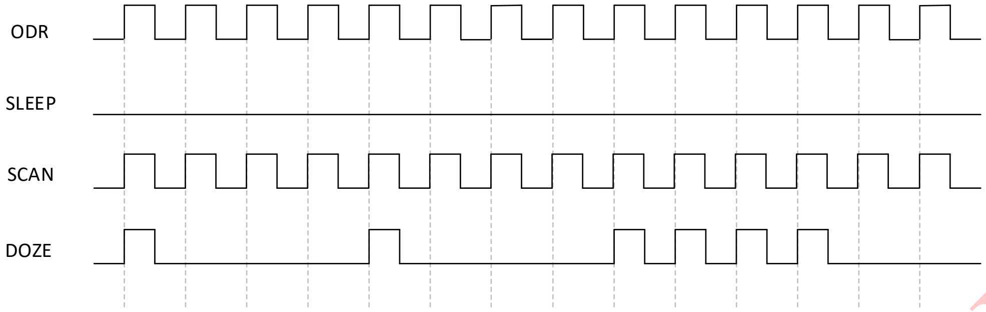


Figure3 Working modes of HX9035

3.4 Timing Diagram

The timing information of HX9035 is as following. The device works under two internal clocks: 32KHz system clock CLK_32K and 5MHz ADC timing clock CLK_5M. The 32KHz clock is running all the time. It controls the scan period configured by register scan_period_i2c. The 5MHz high frequency clock is enabled in scan mode or doze mode. It is used to generate the timing during each conversion.

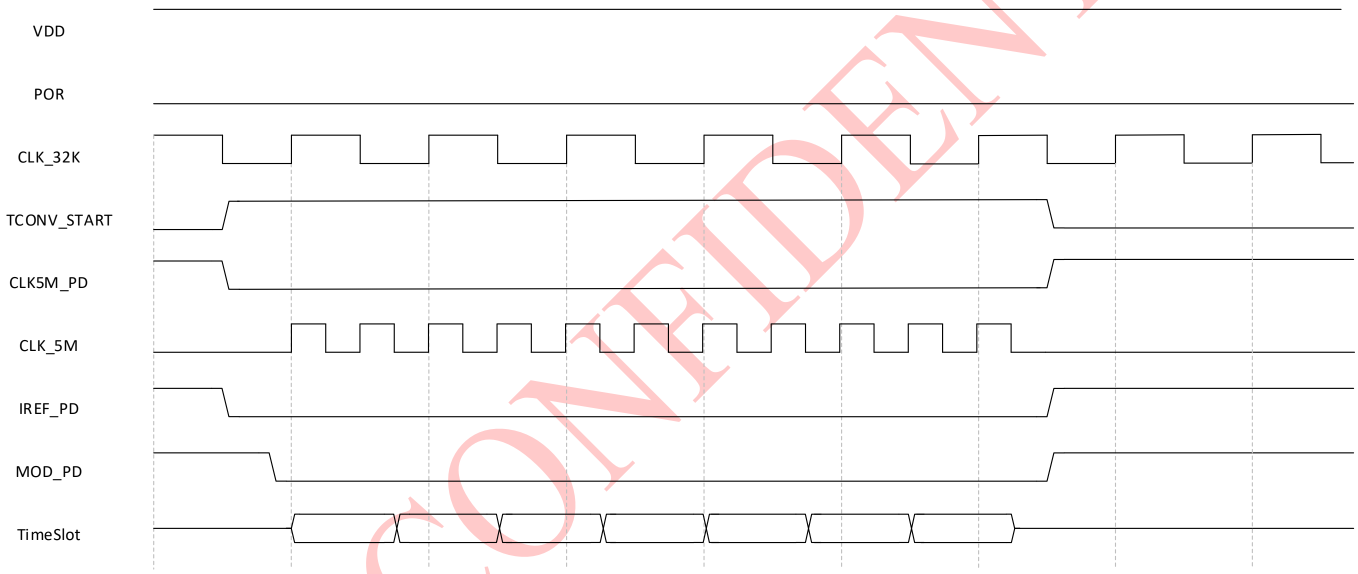


Figure4 Main Timing Diagram

3.5 Analog-to-Digital Converter (ADC)

A delta-sigma ADC is used to convert the input capacitance to a 24bit digital data. The ADC is highly configurable, user can configure the sample frequency, OSR, average time according the application.

The OSR and average number of each channel can be flexible configured through register. This can help the customer optimized the chip performance according different application environment.

Chx_avg_num_i2c: controls the average number of each channel. The down sample filter will output one data after averaged by NAVG times, this will improve the noise performance.

Chx_osr_num_i2c: controls the OSR of the ADC, the OSR can be configured as 64/128/256, depending on the noise and resolution requirement.

Range_i2c: the full scale of the measurement can be configured separately for each channel. The full scale can be configured as 1.25pF/2.5pF/3.75pF/5pF/10pF depending on the application.

3.6 Offset Capacitance Compensation

The offset compensation scheme is used to compensate the capacitance of the sensor to the environment, i.e. PCB board. After the compensation, only the Cuser is feed into the ADC. HX9035 can compensate up to 800pF parasitic cap. The offset cap calibration will be performed before the first measurement and after the calibration, the offset value will be stored into register for each channel.

There are three sources that will trigger the compensation: 1. The compensation will be required when any of the channel is enabled. The compensation is performed before the first measurement. 2. The compensation can be trigger by the user writing a 1 to offset_cali_en_i2c. The offset calibration engine will start right before the next scan period. 3. The DSP will continuously monitor the drift of the Cbulk, when the drift exceeds a certain level preset by the user, the offset calibration scheme will be performed.

The compensation request flag can be set anytime but the compensation scheme will be performed at the beginning of next scan period to keep all parameters coherent. Also, when compensation occurs, all the data in the low pass filter will be reset.

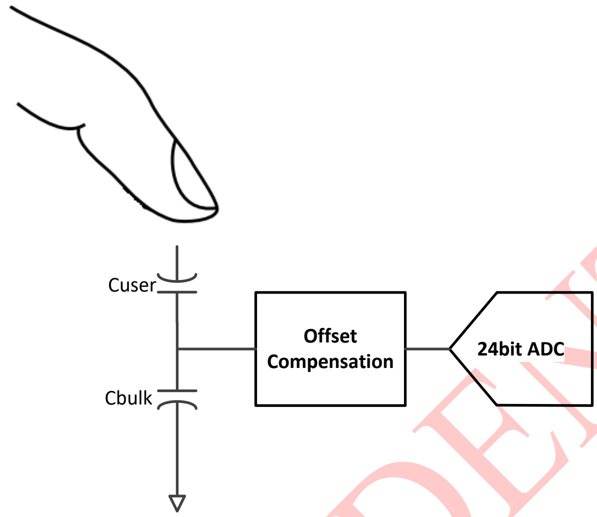


Figure5 Offset Compensation

3.7 Digital Signal Processing

The Digital Signal Processing (DSP) block is incorporated to convert the raw_data from the delta-sigma ADC to a low noise, environment robust prox_diff data which is used to indicate whether a proximity occurs. The offset calibration is performed once before the first measurement. But the environment will vary all the time, the Cbulk will drift along time. The DSP block will continuously monitor the environment drift and filter out the drift to get an environment insensitive prox_diff data.

Figure6 shows the digital processing sequence, after wake up, the digital will repeatedly update the raw_data, prox_diff, pros_stat of each channel.

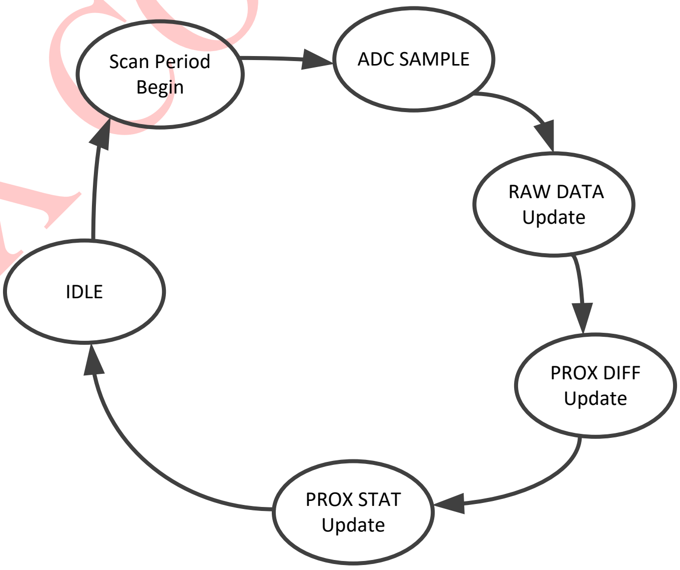


Figure6 Digital Processing Sequence

4 Register Map

Address	Name	R/W	BIT	Function	Default
0x01	DEVICE_ID	RO	<7:0>	Device Identification	0x2E
0x03	CH_NUM_CFG	RW	<5:0>	Conversion phase enable register [CH4~CH0] phase enable register	0x00
0x0D	RAW_BL_CH0_0	RO	<7:0>		0x00
0x0E	RAW_BL_CH0_1	RO	<7:0>	CH0 RAW_DATA/BL_DATA, 24bit width.	0x00
0x0F	RAW_BL_CH0_2	RO	<7:0>		0x00
0x10	RAW_BL_CH1_0	RO	<7:0>		0x00
0x11	RAW_BL_CH1_1	RO	<7:0>	CH1 RAW_DATA/BL_DATA, 24bit width.	0x00
0x12	RAW_BL_CH1_2	RO	<7:0>		0x00
0x13	RAW_BL_CH2_0	RO	<7:0>		0x00
0x14	RAW_BL_CH2_1	RO	<7:0>	CH2 RAW_DATA/BL_DATA, 24bit width.	0x00
0x15	RAW_BL_CH2_2	RO	<7:0>		0x00
0x16	RAW_BL_CH3_0	RO	<7:0>		0x00
0x17	RAW_BL_CH3_1	RO	<7:0>	CH3 RAW_DATA/BL_DATA, 24bit width.	0x00
0x18	RAW_BL_CH3_2	RO	<7:0>		0x00
0x19	RAW_BL_CH4_0	RO	<7:0>		0x00
0x1A	RAW_BL_CH4_1	RO	<7:0>	CH4 RAW_DATA/BL_DATA, 24bit width.	0x00
0x1B	RAW_BL_CH4_2	RO	<7:0>		0x00
0x25	LP_DIFF_CH0_0	RO	<7:0>		0x00
0x26	LP_DIFF_CH0_1	RO	<7:0>	CH0 LP_DATA/DIFF_DATA, 24bit width.	0x00
0x27	LP_DIFF_CH0_2	RO	<7:0>		0x00
0x28	LP_DIFF_CH1_0	RO	<7:0>		0x00
0x29	LP_DIFF_CH1_1	RO	<7:0>	CH1 LP_DATA/DIFF_DATA, 24bit width.	0x00
0x2A	LP_DIFF_CH1_2	RO	<7:0>		0x00
0x2B	LP_DIFF_CH2_0	RO	<7:0>		0x00
0x2C	LP_DIFF_CH2_1	RO	<7:0>	CH2 LP_DATA/DIFF_DATA, 24bit width.	0x00
0x2D	LP_DIFF_CH2_2	RO	<7:0>		0x00
0x2E	LP_DIFF_CH3_0	RO	<7:0>		0x00
0x2F	LP_DIFF_CH3_1	RO	<7:0>	CH3 LP_DATA/DIFF_DATA, 24bit width.	0x00
0x30	LP_DIFF_CH3_2	RO	<7:0>		0x00
0x31	LP_DIFF_CH4_0	RO	<7:0>		0x00
0x32	LP_DIFF_CH4_1	RO	<7:0>	CH4 LP_DATA/DIFF_DATA, 24bit width.	0x00
0x33	LP_DIFF_CH4_2	RO	<7:0>		0x00
0x3E	TS_CFG0	RW	<5:0>	sample frequency of temperature ADC 010100: 1MHz 010110: 909KHz 011000: 833KHz 011010: 769KHz 011100: 714KHz 011110: 666KHz default 100000: 625KHz 100010: 588KHz 100100: 555KHz 100110: 526KHz 101000: 500KHz	0x5E
0x3F	TS_CFG1	RW	<7>	Disable temperature ADC when set 1.	0x92
			<6:4>	Defines the avg num of temperature ADC 000: AVG = 1 001: AVG = 2 default 010: AVG = 4 011: AVG = 8 100: AVG = 16 101: AVG = 32	
			<2:0>	Defines the osr num of temperature ADC 000: OSR = 16 001: OSR = 32 010: OSR = 64 default 011: OSR = 128 100: OSR = 256	

0x40	PRF_CFG	RW	<4:0>	Defines the unit scan period 00000: Min (no idle time) 00001: 2ms 00010: 4ms 00011: 6ms 00100: 8ms 00101: 10ms 00110: 14ms 00111: 18ms 01000: 22ms 01001: 26ms 01010: 30ms 01011: 34ms 01100: 38ms 01101: 42ms 01110: 46ms 01111: 50ms 10000: 56ms 10001: 62ms 10010: 68ms 10011: 74ms 10100: 80ms 10101: 90ms 10110: 100ms 10111: 200ms default 11000: 300ms 11001: 400ms 11010: 600ms 11011: 800ms 11100: 1s 11101: 2s 11110: 3s 11111: 4s	0x17
0x41	CH10_SCAN_FACTOR	RW	<7:4>	Defines the scan factor of conversion phase CH1 000: 1 001: 2 010: 4 011: 8 100: 16 101: 32 110: 64 The real scan period is of CH1 can be calculated by scan factor times unit_scan_period defined by register PRF_CFG	0x00
			<3:0>	Defines the scan factor of conversion phase CH0 000: 1 001: 2 010: 4 011: 8 100: 16 101: 32 110: 64 The real scan period is of CH0 can be calculated by scan factor times unit_scan_period defined by register PRF_CFG	
0x42	CH32_SCAN_FACTOR	RW	<7:4>	Defines the scan factor of conversion phase CH3 000: 1 001: 2 010: 4 011: 8 100: 16 101: 32 110: 64 The real scan period is of CH3 can be calculated by scan factor times unit_scan_period defined by register PRF_CFG	0x00

			<3:0>	Defines the scan factor of conversion phase CH2 000: 1 001: 2 010: 4 011: 8 100: 16 101: 32 110: 64 The real scan period is of CH2 can be calculated by scan factor times unit_scan_period defined by register PRF_CFG	
0x43	CH54_SCAN_FACTOR	RW	<3:0>	Defines the scan factor of conversion phase CH4 000: 1 001: 2 010: 4 011: 8 100: 16 101: 32 110: 64 The real scan period is of CH4 can be calculated by scan factor times unit_scan_period defined by register PRF_CFG	0x00
0x45	CH10_DOZE_FACTOR	RW	<7>	Enables the Doze mode of CH1	0x00
			<6:4>	Defines the scan period enlarge time of CH1 when CH1 is in Doze mode 000: 2X 001: 4X 010: 8X 011: 16X	
			<3>	Enables the Doze mode of CH0	
			<2:0>	Defines the scan period enlarge time of CH0 when CH0 is in Doze mode 000: 2X 001: 4X 010: 8X 011: 16X	
0x46	CH32_DOZE_FACTOR	RW	<7>	Enables the Doze mode of CH3	0x00
			<6:4>	Defines the scan period enlarge time of CH3 when CH3 is in Doze mode 000: 2X 001: 4X 010: 8X 011: 16X	
			<3>	Enables the Doze mode of CH2	
			<2:0>	Defines the scan period enlarge time of CH2 when CH2 is in Doze mode 000: 2X 001: 4X 010: 8X 011: 16X	
0x47	CH54_DOZE_FACTOR	RW	<3>	Enables the Doze mode of CH4	0x00
			<2:0>	Defines the scan period enlarge time of CH4 when CH4 is in Doze mode 000: 2X 001: 4X 010: 8X 011: 16X	
0x49	CH10_PROX_RELEASE_FACTOR	RW	<3:0>	When configured in Doze mode, CH0 will enter into slow conversion mode after several scan period. 0000: 16x scanperiod 0001: 32x 0010: 64x 0011: 128x 0100: 160x 0101: 192x	0x00

				0110: 256x 0111: 320x 1000: 384x 1001: 468x 1010: 512x 1011: 576x 1100: 640x 1101: 704x 1110: 768x 1111: 832x	
0x4E	TC_NOSR_CFG0	RW	<6:4>	Defines the osr of the ADC during CH1 000: OSR = 16 001: OSR = 32 010: OSR = 64 default 011: OSR = 128 100: OSR = 256	0x22
			<2:0>	Defines the osr of the ADC during CH0 000: OSR = 16 001: OSR = 32 010: OSR = 64 default 011: OSR = 128 100: OSR = 256	
0x4F	TC_NOSR_CFG1	RW	<6:4>	Defines the osr of the ADC during CH3 000: OSR = 16 001: OSR = 32 010: OSR = 64 default 011: OSR = 128 100: OSR = 256	0x22
			<2:0>	Defines the osr of the ADC during CH2 000: OSR = 16 001: OSR = 32 010: OSR = 64 default 011: OSR = 128 100: OSR = 256	
0x50	TC_NOSR_CFG2	RW	<2:0>	Defines the osr of the ADC during CH4 000: OSR = 16 001: OSR = 32 010: OSR = 64 default 011: OSR = 128 100: OSR = 256	0x22
0x52	TC_AVG_CFG0	RW	<6:4>	Defines the avg num of the ADC during CH1 000: AVG = 1 001: AVG = 2 default 010: AVG = 4 011: AVG = 8 100: AVG = 16 101: AVG = 32	0x11
			<2:0>	Defines the osr of the ADC during CH0 000: AVG = 1 001: AVG = 2 default 010: AVG = 4 011: AVG = 8 100: AVG = 16 101: AVG = 32	
0x53	TC_AVG_CFG1	RW	<6:4>	Defines the avg num of the ADC during CH3 000: AVG = 1 001: AVG = 2 default 010: AVG = 4 011: AVG = 8 100: AVG = 16 101: AVG = 32	0x11
			<2:0>	Defines the osr of the ADC during CH2 000: AVG = 1	

				001: AVG = 2 default 010: AVG = 4 011: AVG = 8 100: AVG = 16 101: AVG = 32	
0x54	TC_AVG_CFG2	RW	<2:0>	Defines the osr of the ADC during CH4 000: AVG = 1 001: AVG = 2 default 010: AVG = 4 011: AVG = 8 100: AVG = 16 101: AVG = 32	0x11
0x56	OFFSET_CALI_CTRL0	RW	<4:0>	Manual offset compensation enable register: Bit[4:0] enables the manual offset compensation of [CH4~CH0]	0x00
0x57	OFFSET_CALI_CTRL1	RW	<4:0>	Force calibration register Bit[4:0] will trigger offset compensation of [CH4~CH0] when set to 1	0x00
0x58	OFFSET_DAC0_0	RW	<7:0>	Indicates the offset capacitance in CH0	0x00
0x59	OFFSET_DAC0_1	RW	<4:0>	The offset DAC is 13bit resolution, with LSB of 26fF.	0x00
0x5A	OFFSET_DAC1_0	RW	<7:0>	Indicates the offset capacitance in CH1	0x00
0x5B	OFFSET_DAC1_1	RW	<4:0>	The offset DAC is 13bit resolution, with LSB of 26fF.	0x00
0x5C	OFFSET_DAC2_0	RW	<7:0>	Indicates the offset capacitance in CH2	0x00
0x5D	OFFSET_DAC2_1	RW	<4:0>	The offset DAC is 13bit resolution, with LSB of 26fF.	0x00
0x5E	OFFSET_DAC3_0	RW	<7:0>	Indicates the offset capacitance in CH3	0x00
0x5F	OFFSET_DAC3_1	RW	<4:0>	The offset DAC is 13bit resolution, with LSB of 26fF.	0x00
0x60	OFFSET_DAC4_0	RW	<7:0>	Indicates the offset capacitance in CH4	0x00
0x61	OFFSET_DAC4_1	RW	<4:0>	The offset DAC is 13bit resolution, with LSB of 26fF.	0x00
0x68	CH0_CFG_0	RW	<7:6>	Defines the connection of CS3 during conversion phase CH0 00: Non connected 01: Shield 10: Negative 11 Positive	0x03
			<5:4>	Defines the connection of CS2 during conversion phase CH0 00: Non connected 01: Shield 10: Negative 11 Positive	
			<3:2>	Defines the connection of CS1 during conversion phase CH0 00: Non connected 01: Shield 10: Negative 11 Positive	
			<1:0>	Defines the connection of CS0 during conversion phase CH0 00: Non connected 01: Shield 10: Negative 11 Positive	
0x69	CH0_CFG_1	RW	<1:0>	Defines the connection of CS4 during conversion phase CH0 00: Non connected 01: Shield 10: Negative 11 Positive	0x00
0x6A	CH1_CFG_0	RW	<7:6>	Defines the connection of CS3 during conversion phase CH1 00: Non connected 01: Shield 10: Negative 11 Positive	0x0C
			<5:4>	Defines the connection of CS2 during conversion phase CH1 00: Non connected 01: Shield 10: Negative 11 Positive	
			<3:2>	Defines the connection of CS1 during conversion phase CH1 00: Non connected 01: Shield 10: Negative 11 Positive	
			<1:0>	Defines the connection of CS0 during conversion phase CH1 00: Non connected 01: Shield 10: Negative 11 Positive	
0x6B	CH1_CFG_1	RW	<1:0>	Defines the connection of CS4 during conversion phase CH1 00: Non connected 01: Shield 10: Negative 11 Positive	0x00
0x6C	CH2_CFG_0	RW	<7:6>	Defines the connection of CS3 during conversion phase CH2 00: Non connected 01: Shield 10: Negative 11 Positive	0x30
			<5:4>	Defines the connection of CS2 during conversion phase CH2 00: Non connected 01: Shield 10: Negative 11 Positive	
			<3:2>	Defines the connection of CS1 during conversion phase CH2 00: Non connected 01: Shield 10: Negative 11 Positive	
			<1:0>	Defines the connection of CS0 during conversion phase CH2 00: Non connected 01: Shield 10: Negative 11 Positive	
0x6D	CH2_CFG_1	RW	<1:0>	Defines the connection of CS4 during conversion phase CH2 00: Non connected 01: Shield 10: Negative 11 Positive	0x00
0x6E	CH3_CFG_0	RW	<7:6>	Defines the connection of CS3 during conversion phase CH3 00: Non connected 01: Shield 10: Negative 11 Positive	0xC0
			<5:4>	Defines the connection of CS2 during conversion phase CH3 00: Non connected 01: Shield 10: Negative 11 Positive	
			<3:2>	Defines the connection of CS1 during conversion phase CH3	

				00: Non connected 01: Shield 10: Negative 11 Positive	
			<1:0>	Defines the connection of CS0 during conversion phase CH3 00: Non connected 01: Shield 10: Negative 11 Positive	
0x6F	CH3_CFG_1	RW	<1:0>	Defines the connection of CS4 during conversion phase CH3 00: Non connected 01: Shield 10: Negative 11 Positive	0x00
0x70	CH4_CFG_0	RW	<7:6>	Defines the connection of CS3 during conversion phase CH4 00: Non connected 01: Shield 10: Negative 11 Positive	0x00
			<5:4>	Defines the connection of CS2 during conversion phase CH4 00: Non connected 01: Shield 10: Negative 11 Positive	
			<3:2>	Defines the connection of CS1 during conversion phase CH4 00: Non connected 01: Shield 10: Negative 11 Positive	
			<1:0>	Defines the connection of CS0 during conversion phase CH4 00: Non connected 01: Shield 10: Negative 11 Positive	
0x71	CH4_CFG_1	RW	<1:0>	Defines the connection of CS4 during conversion phase CH4 00: Non connected 01: Shield 10: Negative 11 Positive	0x03
0x77	CH7_CFG_0	RW	<7:6>	Defines the connection of CS3 during conversion phase CH7 00: Non connected 01: Shield 10: Negative 11 Positive	0x00
			<5:4>	Defines the connection of CS2 during conversion phase CH7 00: Non connected 01: Shield 10: Negative 11 Positive	
			<3:2>	Defines the connection of CS1 during conversion phase CH7 00: Non connected 01: Shield 10: Negative 11 Positive	
			<1:0>	Defines the connection of CS0 during conversion phase CH7 00: Non connected 01: Shield 10: Negative 11 Positive	
0x78	RANGE_CFG_0	RW	<6:4>	Defines the measurement fullscale during conversion phase CH1 000: 1.25pF default 001: 2.5pF 010: 3.75pF 011: 5pF 100: 6.25pF 101: 7.5pF 110: 8.75pF 111: 10pF	0x00
			<2:0>	Defines the measurement fullscale during conversion phase CH0 000: 1.25pF default 001: 2.5pF 010: 3.75pF 011: 5pF 100: 6.25pF 101: 7.5pF 110: 8.75pF 111: 10pF	
0x79	RANGE_CFG_1	RW	<6:4>	Defines the measurement fullscale during conversion phase CH3 000: 1.25pF default 001: 2.5pF 010: 3.75pF 011: 5pF 100: 6.25pF 101: 7.5pF 110: 8.75pF 111: 10pF	0x00
			<2:0>	Defines the measurement fullscale during conversion phase CH2 000: 1.25pF default 001: 2.5pF 010: 3.75pF 011: 5pF 100: 6.25pF 101: 7.5pF 110: 8.75pF	

				111: 10pF	
0x7A	RANGE_CFG_2	RW	<2:0>	Defines the measurement fullscale during conversion phase CH4 000: 1.25pF default 001: 2.5pF 010: 3.75pF 011: 5pF 100: 6.25pF 101: 7.5pF 110-: 8.75pF 111: 10pF	0x00
0x9A	DSP_CONFIG_CTRL7	RW	<4:0>	Defines the output data of RA_LP_DIFF_CH<4:0> register, each bit for one phase, 0 for LP_DATA, 1 for DIFF_DATA	0xFF
0x9B	DSP_CONFIG_CTRL8	RW	<4:0>	Defines the output data of RA_RAW_BL_CH<4:0> register, each bit for one phase, 0 for RAW_DATA, 1 for BL_DATA	0xFF
0x9C	DSP_CONFIG_CTRL9	RW	<7:4>	If the baseline data exceeds the threshold, the corresponding conversion phase will be auto calibrated. The threshold is defined as: 0001: 2048 0010: 4096 … … 1000: 14336 default … … 1111 32768	0x70
0xA0	INTERRUPT_CFG0	RW	<7>	Enable the interrupt if the offset calibration is finished.	0x80
			<6>	Defines the polarity of interrupt, 0 for active low 1 for active high	
			<3>	Defines the interrupt type, 0 for pulse, 1 for level	
0xA1	INTERRUPT_CFG1	RW	<4:0>	The conversion ready interrupt for conversion phase <CH4~CH0> will be enabled if the bit is set to 1.	0x00
0xA2	INTERRUPT_CFG2	RW	<4:0>	The first level far interrupt will be enabled for conversion phase < CH4~CH0> if the bit is set to 1.	0xFF
0xA3	INTERRUPT_CFG3	RW	<4:0>	The second level far interrupt will be enabled for conversion phase < CH4~CH0> if the bit is set to 1.	0x00
0xA4	INTERRUPT_CFG4	RW	<4:0>	The third level far interrupt will be enabled for conversion phase < CH4~CH0 if the bit is set to 1.	0x00
0xA5	INTERRUPT_CFG5	RW	<4:0>	The first level near interrupt will be enabled for conversion phase < CH4~CH0> if the bit is set to 1.	0xFF
0xA6	INTERRUPT_CFG6	RW	<4:0>	The second level near interrupt will be enabled for conversion phase < CH4~CH0> if the bit is set to 1.	0x00
0xA7	INTERRUPT_CFG7	RW	<4:0>	The third level near interrupt will be enabled for conversion phase < CH4~CH0> if the bit is set to 1.	0x00
0xAB	PROX_INT_CFG	RW	<7:4>	A near interrupt will be enabled if the DIFF_DATA reaches the threshold for several time consecutively. 0001: 1 time 0010: 2 times … … 1110: 14 times 1111: 15 times	0x11
			<3:0>	A far interrupt will be enabled if the DIFF_DATA reaches the threshold for several time consecutively. 0001: 1 time 0010: 2 times … … 1110: 14 times 1111: 15 times	
0xAC	BL_UP_CFG0	RW	<7:4>	Defines the up coefficient of the first order baseline filter during CH1. 0000: 0 0001: 1 0010: 1/2 0011: 1/4	0x99

				0100: 1/8 0101: 1/16 0110: 1/32 0111: 1/64 1000: 1/128 1001: 1/256 default 1010: 1/512	
			<3:0>	Defines the up coefficient of the first order baseline filter during CH0. 0000: 0 0001: 1 0010: 1/2 0011: 1/4 0100: 1/8 0101: 1/16 0110: 1/32 0111: 1/64 1000: 1/128 1001: 1/256 default 1010: 1/512	
0xAD	BL_UP_CFG1	RW	<7:4>	Defines the up coefficient of the first order baseline filter during CH3. 0000: 0 0001: 1 0010: 1/2 0011: 1/4 0100: 1/8 0101: 1/16 0110: 1/32 0111: 1/64 1000: 1/128 1001: 1/256 default 1010: 1/512	0x99
			<3:0>	Defines the up coefficient of the first order baseline filter during CH2. 0000: 0 0001: 1 0010: 1/2 0011: 1/4 0100: 1/8 0101: 1/16 0110: 1/32 0111: 1/64 1000: 1/128 1001: 1/256 default 1010: 1/512	
0xAE	BL_UP_CFG2	RW	<3:0>	Defines the up coefficient of the first order baseline filter during CH4. 0000: 0 0001: 1 0010: 1/2 0011: 1/4 0100: 1/8 0101: 1/16 0110: 1/32 0111: 1/64 1000: 1/128 1001: 1/256 default 1010: 1/512	0x99
0xB0	BL_DN_CFG0	RW	<7:4>	Defines the dn coefficient of the first order baseline filter during CH1. 0000: 0 0001: 1	0x11

				0010: 1/2 0011: 1/4 0100: 1/8 0101: 1/16 0110: 1/32 0111: 1/64 1000: 1/128 1001: 1/256 default 1010: 1/512	
			<3:0>	Defines the dn coefficient of the first order baseline filter during CH0. 0000: 0 0001: 1 0010: 1/2 0011: 1/4 0100: 1/8 0101: 1/16 0110: 1/32 0111: 1/64 1000: 1/128 1001: 1/256 default 1010: 1/512	
0xB1	BL_DN_CFG1	RW	<7:4>	Defines the dn coefficient of the first order baseline filter during CH3. 0000: 0 0001: 1 0010: 1/2 0011: 1/4 0100: 1/8 0101: 1/16 0110: 1/32 0111: 1/64 1000: 1/128 1001: 1/256 default 1010: 1/512	0x11
			<3:0>	Defines the dn coefficient of the first order baseline filter during CH2. 0000: 0 0001: 1 0010: 1/2 0011: 1/4 0100: 1/8 0101: 1/16 0110: 1/32 0111: 1/64 1000: 1/128 1001: 1/256 default 1010: 1/512	
0xB2	BL_DN_CFG2	RW	<3:0>	Defines the dn coefficient of the first order baseline filter during CH4. 0000: 0 0001: 1 0010: 1/2 0011: 1/4 0100: 1/8 0101: 1/16 0110: 1/32 0111: 1/64 1000: 1/128 1001: 1/256 default 1010: 1/512	0x11
0xB5	LP_ALP_CFG0	RW	<6:4>	Defines the coefficient of the first order low pass filter during CH1.	0x00

				000: 1 default 001: 1/2 010: 1/4 011: 1/8 100: 1/16 101: 1/32 110: 1/64	
			<2:0>	Defines the coefficient of the first order low pass filter during CH0. 000: 1 default 001: 1/2 010: 1/4 011: 1/8 100: 1/16 101: 1/32 110: 1/64	
0xB6	LP_ALP_CFG1	RW	<6:4>	Defines the coefficient of the first order low pass filter during CH3. 000: 1 default 001: 1/2 010: 1/4 011: 1/8 100: 1/16 101: 1/32 110: 1/64	0x00
			<2:0>	Defines the coefficient of the first order low pass filter during CH2. 000: 1 default 001: 1/2 010: 1/4 011: 1/8 100: 1/16 101: 1/32 110: 1/64	
0xB7	LP_ALP_CFG2	RW	<2:0>	Defines the coefficient of the first order low pass filter during CH4. 000: 1 default 001: 1/2 010: 1/4 011: 1/8 100: 1/16 101: 1/32 110: 1/64	0x00
0xB9	CH0_COE_CFG_0	RW	<6:0>	Defines the digital gain of conversion phase CH0 0x01 1/64 0x40 64/64 0x41 65/64 0x42 66/64 … … 0x4d 125/64 0x4e 126/64 0x7f 127/64	0x40
0xBB	CH1_COE_CFG_0	RW	<6:0>	Defines the digital gain of conversion phase CH1 0x01 1/64 0x40 64/64 0x41 65/64 0x42 66/64 … … 0x4d 125/64 0x4e 126/64 0x7f 127/64	0x40

<table>
<tr><td>0xBD</td><td>CH2_COE_CFG_0</td><td>RW</td><td><6:0></td><td>Defines the digital gain of conversion phase CH2
0x001: 1/512
0x01 1/64
0x40 64/64
0x41 65/64
0x42 66/64
… …
0x4d 125/64
0x4e 126/64
0x7f 127/64</td><td>0x40</td></tr>
<tr><td>0xBF</td><td>CH3_COE_CFG_0</td><td>RW</td><td><6:0></td><td>Defines the digital gain of conversion phase CH3
0x01 1/64
0x40 64/64
0x41 65/64
0x42 66/64
… …
0x4d 125/64
0x4e 126/64
0x7f 127/64</td><td>0x40</td></tr>
<tr><td>0xC1</td><td>CH4_COE_CFG_0</td><td>RW</td><td><6:0></td><td>Defines the digital gain of conversion phase CH4
0x01 1/64
0x40 64/64
0x41 65/64
0x42 66/64
… …
0x4d 125/64
0x4e 126/64
0x7f 127/64</td><td>0x40</td></tr>
<tr><td>0xC9</td><td>PROX_HIGH_THRES1_CFG0</td><td>RW</td><td><5:0></td><td rowspan="5">The Registers define the first level near threshold of [CH4 ~ CH0], 5bit control for each phase. The threshold is defined as:
00000: 128
00001: 144
00010: 160
00011: 176
00100: 192
00101: 208
00110: 224
00111: 240
01000: 256
01001: 320
01010: 384
01011: 448
01100: 512
01101: 640
01110: 768
01111: 896
10000: 1024
10001: 1280
10010: 1536
10011: 1792
10100: 2048
10101: 2560
10110: 3072
10111: 3584
11000: 4096
11001: 5120
11010: 6144
11011: 7168
11100: 8192
11101: 12288
11110: 16384
11111: 24576</td><td>0x0C</td></tr>
<tr><td>0xCA</td><td>PROX_HIGH_THRES1_CFG1</td><td>RW</td><td><5:0></td><td>0x0C</td></tr>
<tr><td>0xCB</td><td>PROX_HIGH_THRES1_CFG2</td><td>RW</td><td><5:0></td><td>0x0C</td></tr>
<tr><td>0xCC</td><td>PROX_HIGH_THRES1_CFG3</td><td>RW</td><td><5:0></td><td>0x0C</td></tr>
<tr><td>0xCD</td><td>PROX_HIGH_THRES1_CFG4</td><td>RW</td><td><5:0></td><td>0x0C</td></tr>
<tr><td>0xD1</td><td>PROX_HIGH_THRES2_CFG0</td><td>RW</td><td><5:0></td><td>The Registers define the second level near threshold of</td><td>0x10</td></tr>
</table>

0xD2	PROX_HIGH_THRES2_CFG1	RW	<5:0>	[CH4~CH0], 5bit control for each phase. The threshold definition is the same with previous registers.	0x10
0xD3	PROX_HIGH_THRES2_CFG2	RW	<5:0>		0x10
0xD4	PROX_HIGH_THRES2_CFG3	RW	<5:0>		0x10
0xD5	PROX_HIGH_THRES2_CFG4	RW	<5:0>		0x10
0xD9	PROX_HIGH_THRES3_CFG0	RW	<5:0>	The Registers define the third level near threshold of [CH4~CH0], 5bit control for each phase. The threshold definition is the same with previous registers.	0x18
0xDA	PROX_HIGH_THRES3_CFG1	RW	<5:0>		0x18
0xDB	PROX_HIGH_THRES3_CFG2	RW	<5:0>		0x18
0xDC	PROX_HIGH_THRES3_CFG3	RW	<5:0>		0x18
0xDD	PROX_HIGH_THRES3_CFG4	RW	<5:0>		0x18
0xE1	DITHER_CFG	RW	<3>	Enable the spread spectrum function if set to 1.	0x01
			<2>	Defines the shape of spread spectrum function, 0 for rectangle, 1 for triangle	
			<1:0>	Defines the strength of spread spectrum 00: 1/8， 01: 1/4， 10: 1/2， 11: 1	
0xE2	SAMPLE_NUM_0	RW	<7:0>	The 10bit register defines the sample frequency of the ADC, the sample frequency can be depicted with below formula: *Fsample = 1.0 / (sample_num * 200ns)*, while the sample_num is the value the register in decimal.	0x32
0xE3	SAMPLE_NUM_1	RW	<1:0>		0x00
0xE4	INTEGRATION_NUM_0	RW	<7:0>	The integration num should be the same with the SAMPLE_NUM.	0x32
0xE5	INTEGRATION_NUM_0	RW	<1:0>		0x00
0xF2	PROX_STATUS1	RO	<4:0>	Indicates the first proximity occurrence of [CH4~CH0]	0x00
0xF3	PROX_STATUS2	RO	<4:0>	Indicates the second proximity occurrence of [CH4~CH0]	0x00
0xF9	PROX_THRES_EN_CFG	RW	<2:0>	Defines which threshold will be used to lock the baseline data. 001: First level threshold 010: Second level threshold 011: Third level threshold	0x01

5 I2C Protocol

5.1 I2C Data format

The I2C bus protocol was developed by Philips (now NXP). The device supports the standard writing and reading protocol. The 7-bit device address is 0x1b. The register index will automatically increase by 1 after the addressed register has been accessed (read or write). And the format is shown as following:

A Acknowledge (0)

P Stop Condition

R Read (1)

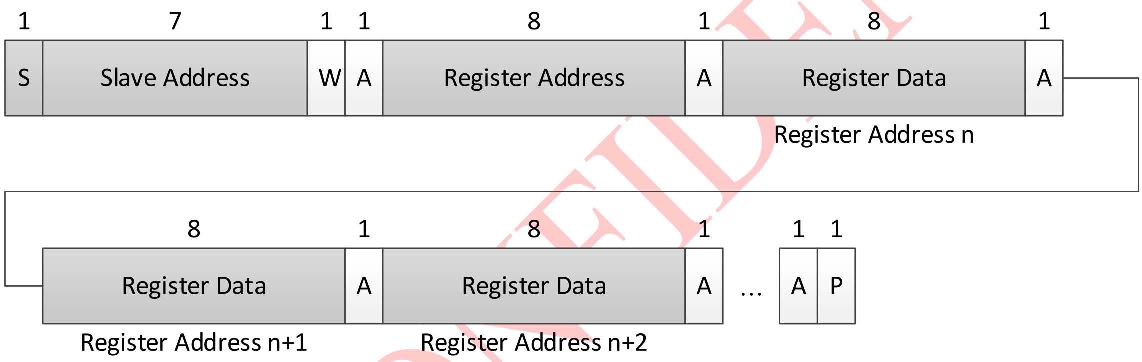
S Start Condition

W Write (0)

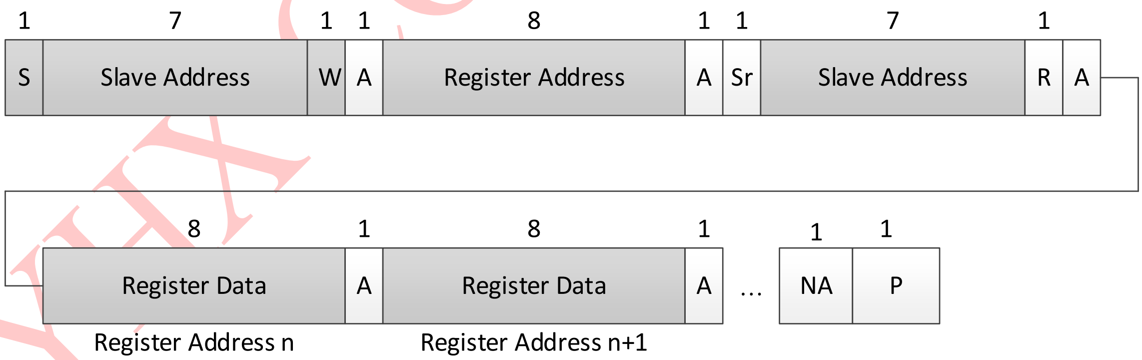
Sr Repeated Start Condition

■Master-to- Slave

□ Slave-to-Master



I2C Write Register Data



I2C Read Register Data

Figure7 I2C data format diagram

5.2 I2C Electrical Characteristics

Table2 I^{2}C Electrical Characteristics

PARAMETER	SYMBOL	STANDARD		FAST		UNIT
		MIN	MAX	MIN	MAX	
LOW level input voltage: fixed input levels VDD-related input levels	VIL	0.5 0.5	1.5 0.3VDD	n/a 0.5	n/a 0.3VDD$^{(1)}$	V V
HIGH level input voltage:	VIH					

fixed input levels VDD-related input levels		3 0.7VDD	Note(2) Note(2)	3 0.7VDD(1)	n/a Note(2)	V V
Hysteresis of Schmitt trigger inputs: VDD > 2 V VDD < 2 V	Vhys	n/a n/a	n/a n/a	0.05VDD 0.1VDD	– –	V V
LOW level output voltage (open drain or open collector) at 3 mA sink current: VDD > 2 V VDD < 2 V	VOL1 VOL2	0 n/a	0.4 n/a	0 0	0.4 0.2VDD	V V
Output fall time from VIHmin to VILmax with a bus capacitance from 10 pF to 400 pF	tof	–	250(4)	20+0.1 Cb(3)	250(4)	ns
Pulse width of spikes which must be suppressed by the input filter	tSP	n/a	n/a	0	50	ns
Input current each I/O pin with an input voltage between 0.1VDD and 0.9VDDmax	Ii	-10	10	-10(5)	10(5)	A
Capacitance for each I/O pin	Ci	-	10	-	10	pF

Notes

1. Devices that use non-standard supply voltage switch don't conform to the intended I2C-bus system levels must relate input levels to the VDD voltage to which the pull-up resistors Rp are connected.
2. Maximum $V_{IH} = V_{DDmax} + 0.5V$.
3. C_b = capacitance of one bus line in pF.
4. The maximum t_f for the SDA and SCL bus lines quoted in Table3(300ns) is longer than the specified maximum t_{of} for the output stages (250 ns). This allows series protection resistors (R_S) to be connected between the SDA/SCL pins and the SDA/SCL bus lines without exceeding the maximum specified tf.
5. I/O pins of Fast-mode devices must not obstruct the SDA and SCL lines if VDD is switched off.

n/a = not applicable

5.3 I2C Timing

The I2C Timing is as following figure:

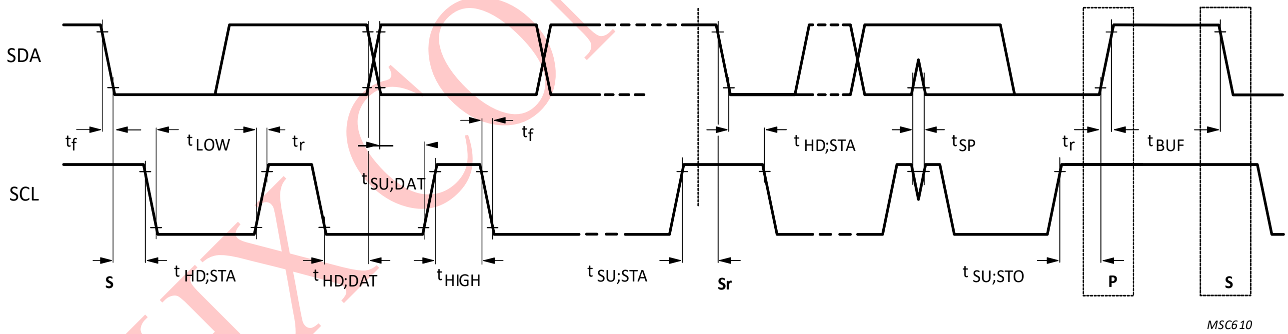


Figure8 I²C Timing

Table3 I²C Timing Parameters(1)

PARAMETER	SYMBOL	MIN	MAX	UNIT
SCL clock frequency	f_{SCL}	0	800	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	0.6	–	us
LOW period of the SCL clock	t_{LOW}	1.3	–	us
HIGH period of the SCL clock	t_{HIGH}	0.6	–	us
Set-up time for a repeated START condition	$t_{SU;STA}$	0.6	–	us
Data hold time	tHD;DAT	0(2)	–	us
Data set-up time	$t_{SU;DAT}$	100(3)	–	ns
Rise time of both SDA and SCL signals	tr	–	300	ns
Fall time of both SDA and SCL signals	tf	–	300	ns

Set-up time for STOP condition	$t_{SU;STO}$	0.6	–	us
Bus free time between a STOP and START condition	t_{BUF}	1.3	–	us
Capacitive load for each bus line	C_b	–	400	pF
Noise margin at the LOW level for each connected device (including hysteresis)	V_{nL}	$0.1V_{DD}$	–	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{nH}	$0.2V_{DD}$	–	V

Notes

1. All values referred to VIHmin and VILmax levels (see Table2).
2. A device must internally provide a hold time of at least 300ns for the SDA signal(referred to the VIHmin of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement tSU;DAT⩾250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line tr max + tSU;DAT = 1000 + 250 = 1250 ns (according to the Standard-mode I2C-bus specification) before the SCL line is released.

6 Application Information

Typical application for HX9035 is showing below:

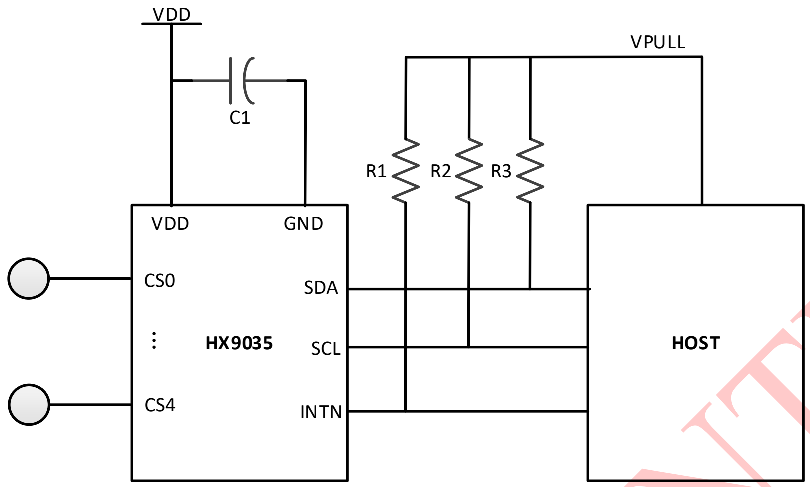


Figure9 Typical Application Schematic

Note:

1. Any CSx pad can be configured as dummy pad and at most five independent channels can be used simultaneously

And the device value is listed below:

Table4 I^2C Timing Parameters

DEVICE NAME	Value	Description
VDD	1.8V	Low noise
VPULL	1.2~3.6V	
C1	1uF	
R1	2.2 KΩ	
R2	2.2 KΩ	
R3	2.2 KΩ	

7 Package Information

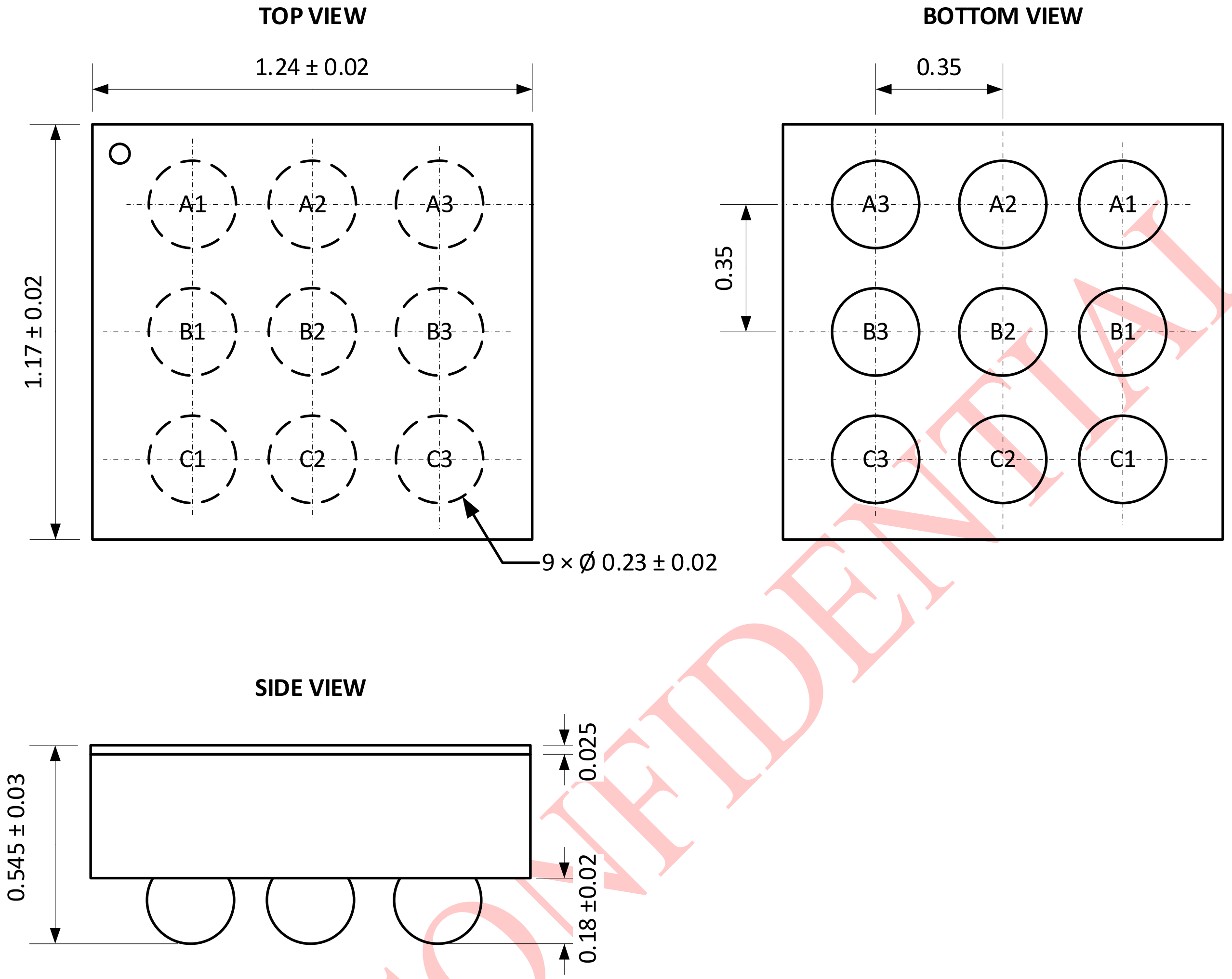


Figure10 Package Information (Unit: mm)

7.1 Land Pattern

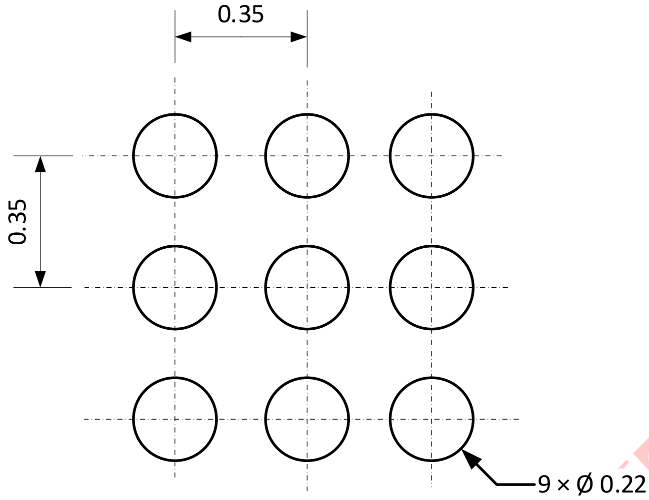


Figure11 Land Pattern

NOTES:

1. Controlling dimensions are in millimeters(angles in degrees).
2. This land pattern is for reference group to ensure your company's manufacturing are met.

8 Soldering Information

The module has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate. The process, equipment, and material used in these tests are detailed below. The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

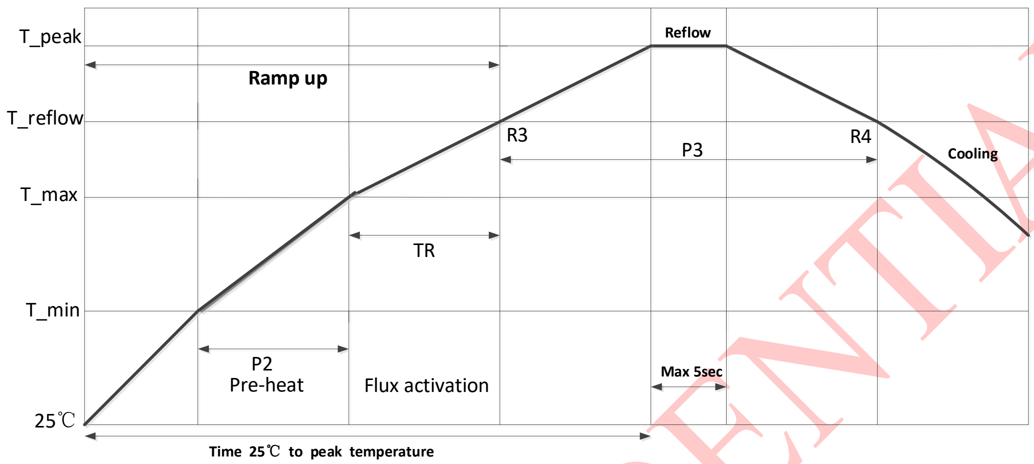


Figure12 Solder reflow profile grape

Table5 Solder Reflow Profile

	Peak temperature (Tpeak)	250-255℃; Max 5sec
Pre-Heat	Temperature min (Tmin)	150℃; 2℃/Sec
	Temperature max(Tmax)	150-217℃； 100S to 180S
	P2：（T min to max）	90-110s
Time maintain above	Temperature (Tre flow)	217℃
	Time (P3)	60-90sec
	R3 Slope (from 217℃ to peak)	2℃/sec(typ) to 2.5℃/sec(max)
	R4 Slope (from peak to 217℃)	1.5℃/sec(typ) to 4℃/sec(max)
	Time to peak temperature	480s Max
	Cooling down slope (peak to 217℃)	2-4℃/sec

REVISION HISTORY

Version	Date	Comment
1.0	Dec 9, 2021	Initial version
1.1	Nov 2, 2021	Modify voltage of host control