HX3229-39B Digital 16bit Ambient Light Sensor

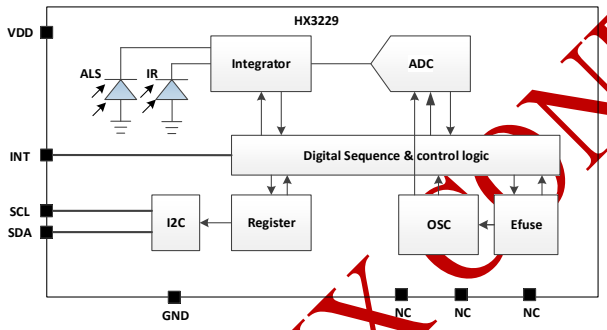
■ Description

HX3229-39B is a high sensitivity and wide range input digital ambient light sensor with I²C bus interface. The ALS sensor can output two channel data, a visible channel data and an IR channel data, to realize backlight and display brightness control.

■ Application

- Mobile Phone, Smartphone
- PDA
- Wearable device

■ Block Diagram



■ Features

- Up to 16 bits ADC for high resolution ALS.
- Ultra-high sensitivity 0.0006lux/count.
- Wide range, flexible and high linear gain control: 1X/2X/……/2048X.
- FOV up to 100° for better performance in dark environment.
- Excellent spectral response similar to human-eye response and suppress IR portion.
- Flexible interrupt setting.
- Typical configuration power consumption：280uA.

■ General

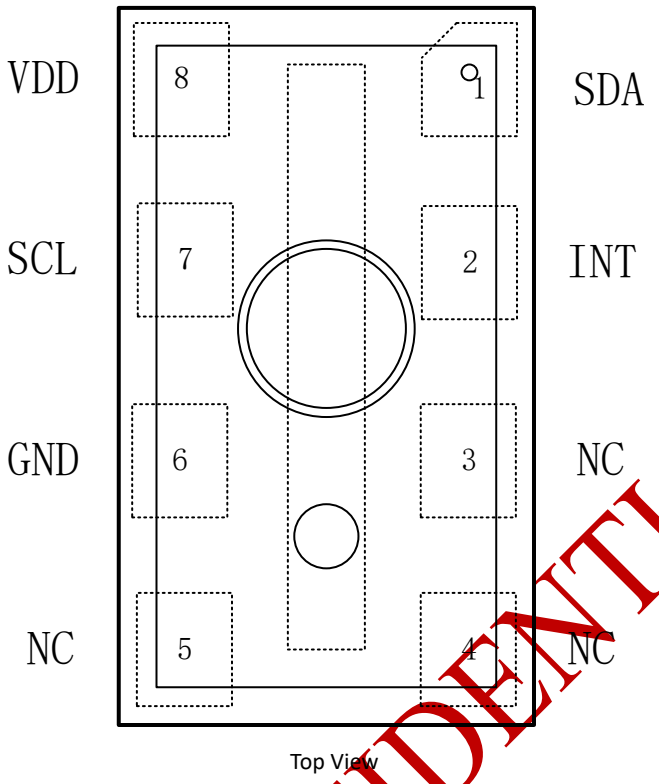
- Fully digital control with I²C interface, 1.7~3.6V I2C interface.
- VDD operation voltage : 2.7~3.6V
- Package :
  HX3229：3.94*2.36*1.35mm.
  HX3229-39B：4.94*3.36*3.9mm.
- Lead-free package (RoHS compliant).
- Moisture Sensitivity Level 3.

Added Value of Using HX3229-39B

Benefits	Features
● Approximates Human Eye Response	● Dual Diode
● Suited for Operation Behind Dark Glass	● Ultra-high sensitivity 0.0006LUX/count
● Low power consumption	● Typical Work Mode @ 280uA ● Sleep Mode @ 1uA

CONTENTS

Pin Configuration



Top View

Pin List

PIN	Name	Type	Description
1	SDA	I/O	Serial data I/O for I²C
2	INT	O	Interrupt outputs, selectable open drain(default) or cmos
3	NC		Do not connect, keep floating
4	NC		Do not connect, keep floating
5	NC		Do not connect, keep floating
6	GND	GND	Power supply ground
7	SCL	I	Clock signal for I²C serial data
8	VDD	PWR	Power supply voltage

Specifications

Absolute Maximum Ratings

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Supply voltage	-	-	3.6	V
V_{IN_MR}	Input voltage [SCL SDA]	-0.3		3.6	V
V_{OUT_MR}	Output voltage [INT]	-0.3		3.6	V
Tstg	Storage temperature	-40	-	85	℃
Tjmax	Maximum Junction Temperature	-	-	100	℃
ESD	ESD tolerance, human body model	±2000			V

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Supply voltage	2.7	3.3	3.6	V
Ta	Operation temperature, functional	-30		85	℃
	Operation temperature, best performance	-20	-	65	℃
V_{IN}	Input voltage [SCL SDA]	1.7	3.3	3.6	V
F_{I2C}	Clock frequency of I2C	-	-	400	KHz

Electrical and Optical Characteristics

Typical specifications are at Ta= 25°C, VDD =3.3V, Gain=1x, ALS 16 bits resolution, INT_TIME=100ms, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
General characteristics					
Power Consumption	ALS input light 100LUX		280		uA
	Power down		0.5	1	uA
ALS characteristics					
ALS_{FSCNT}	Full scale ALS counts			65535	Counts
λ_{P1}	Peak sensitivity wavelength for ALS		550		nm
ALS Range	Gain=1X	0		72K	Lux
ALS Dark Offset	No input light		0	3	Count
CH0 data count value	Ev=1000LUX White LED is used	1020	1200	1380	Count
CH1 data count value	Ev=1000LUX White LED is used	0	5	10	Count
ALS Gain		1		2048	
Measurement Time		94	100	106	ms
FOV			100		deg
CLK (Internal 1.31MHz Oscillator)					
Frequency			1.31		MHz
I^2C INTERFACE					
Maximum Clock Speed				400	KHz
I2C Slave Address			0x44		

Detailed Description

Overview

HX3229-39B is a high resolution digital ambient light sensor (ALS) in a single 8-pin package. HX3229-39B includes two photo-diodes, digital state machine, wide range gain control and very low noise ADC in a single chip. The excellent spectral response is designed to be close to human eye. With 1X to 2048X gain, HX3229-39B is suitable for detecting a wide range of light intensity environment. Software shutdown mode control is provided for low power application.

Functional Block Diagram

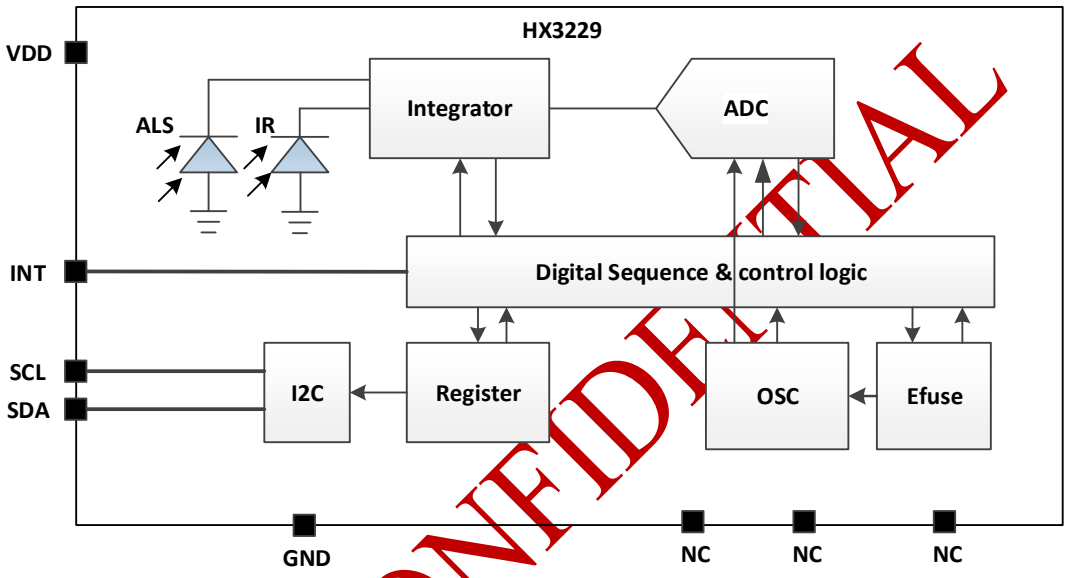


Figure1 Functional Block Diagram

Digital State Machine Diagram

The running state machine of ALS is as shown in Figure2. The HX3229-39B has mainly three modes of operation.
In Sleep mode: configured by the Power Down (PD) register. All circuits except I2C are turned off and consume very low current.
In normal mode (ALS): all circuits are working.
In standby mode (PRF wait): all circuits except the I2C and 32KHz clocks are turned off to save power.

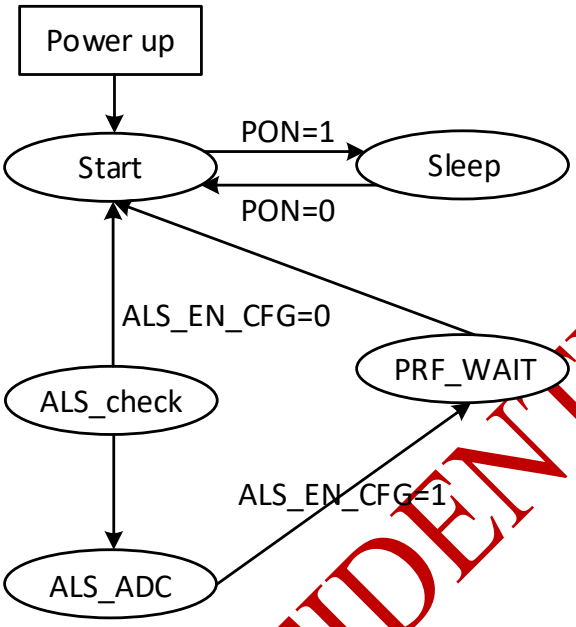


Figure2 State Machine Diagram

ALS operation

ALS curve in typical configuration

Typical specifications are at 25°C. VDD=3.3V, Gain=64X and 16X, ALS 16 bits resolution, The ALS curve of the HX3229-39B is shown in the following figure.

Figure3 Typical ALS curve

FOV

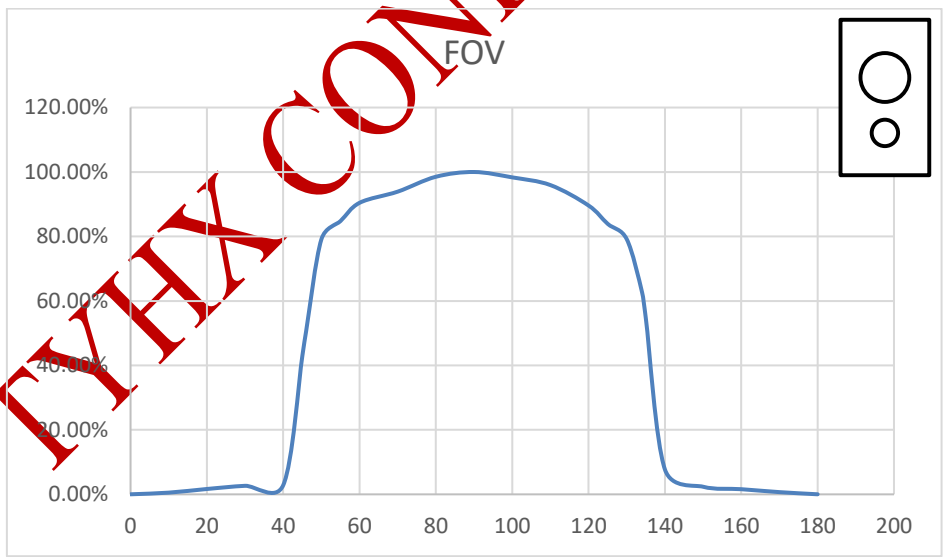


Figure4 vertical FOV

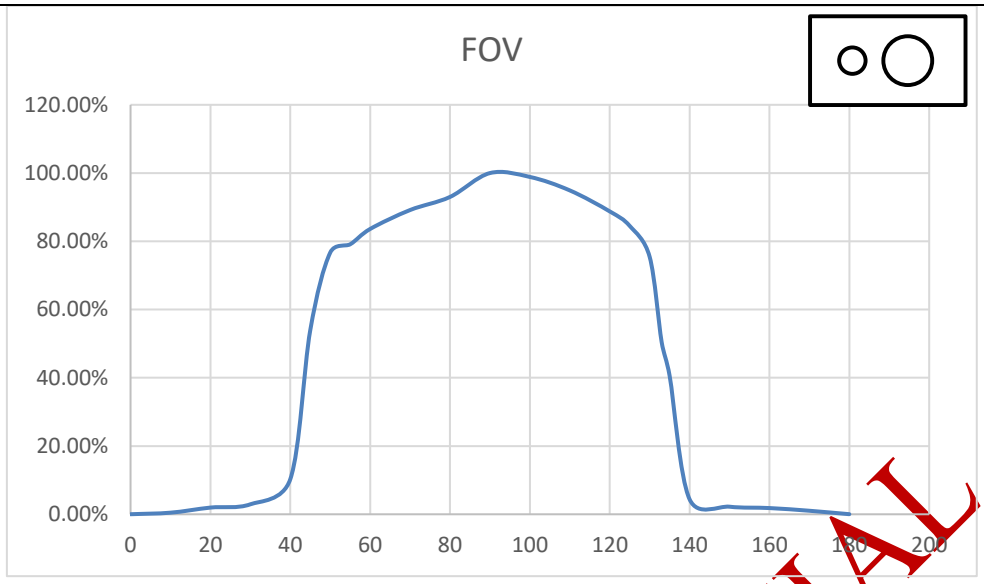


Figure5 transverse FOV

ALS response curve

The PD corresponding to the ALS was coated, and the PD response curve after coating was as shown.

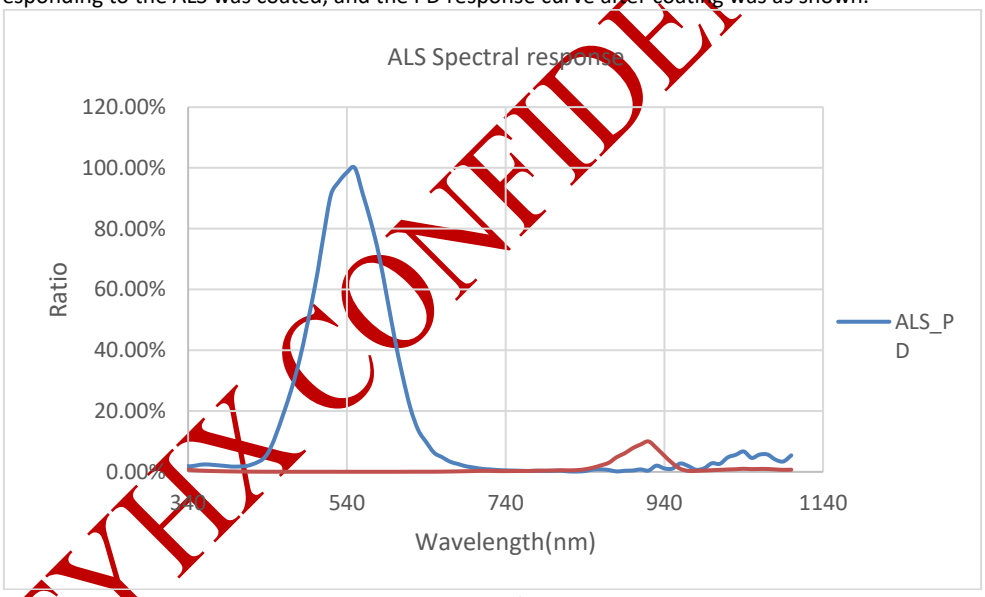


Figure6 Spectral Response

Register Map

Address	Name	R/W	Function	Default
0x00	ID	RO	RA_PART_ID	0x25
0x01	ALS _ENABLE	RW	ALS enable	0x11
0x02	PD_SEL	RW	PD selection	0x37
0x05	INT_CTRL0	RW	Interrupt control	0xff
0x06	INT_CTRL1	RW	Interrupt control	0x41
0x07	INT_CTRL2	RW	Interrupt control	0x00
0x0F	PRF_CTRL	RW	PRF control, bits [7:0]	0xFF
0x10		RW	PRF control, bits [15:8]	0xFF
0x11		RW	PRF control, bits [21:16]	0x3F
0x12	TH_CTRL	RW	High threshold, bits [7:0]	0xFF
0x13		RW	High threshold, bits [15:0]	0xFF
0x14	TL_CTRL	RW	Low threshold, bits [7:0]	0x00
0x15		RW	Low threshold, bits [15:0]	0x00
0x16	ADCGAIN_ADC_RST_CTRL	RW	ADC GAIN ADC reset width control	0x00
0x17	CURGAIN_CTRL	RW	CURGAIN control	0x08
0x18	ALS INTERVAL	RW	ALS phase3 interval control	0x02
0x19	ADC INTCAPSEL ALS	RW	ALS INTCAPSEL	0x7F
0xA4	DATA0	RO	Data0 out, bits [7:0]	0x00
0xA5		RO	Data0 out, bits [15:8]	0x00
0xA6	DATA1	RO	Data1 out, bits [7:0]	0x00
0xA7		RO	Data1 out, bits [15:8]	0x00
0xC1	ADC range	RW	ADC range select	0x85
0xC7	ADC mode	RW	ADC NRZ mode enable	0x00

Init Register Map

Address	Default	Name	configuration
0x01	0x11	ALS_ENABLE	0xC0
0x07	0x00	INT_CTRL2	0X41
0x0F	0xFF	PRF_CTRL	0x00
0x10	0xFF		0x30
0x11	0x3F		0x02
0x16	0x00	ADCGAIN_ADC_RST_CTRL	0x23
0x17	0x08	CURGAIN_CTRL	0x08
0x19	0x7F	ADCINTCAPSEL	0xFF
0xC1	0x85	ADC range select	0x55
0xC7	0x00	ADC NRZ mode enable	0XA0

Register Description

Register(0x00)

Address	Type	Default	Name	BIT	Default	Description
0x00	RO	0x25	ID	7:0	25	HX3229-39B chip ID

Register(0x01)

Address	Type	Default	Name	BIT	Default	Description
0x01	RW	0x11	ALS_EN_I2C	7	0	1: ALS function enable 0: ALS function disable
			INTTIME	6:4	001	ADC Full code 1code=1/(1.31MHZ) 000: 4095 001: 8191 010: 16383 011: 32767 100: 65535 101: 65535, average 2 times 110: 65535, average 4 times 111: 65535, average 8 times
			RESERV	3	0	RESERV
			RESERV	2:0	001	RESERV

Register(0x02)

Address	Type	Default	Name	BIT	Default	Description
0x02	RW	0x37	RESERVE	7	0	RESERVE
			INTPDSEL_ ALS1_I2C	6	0	Selection of ALS phase1 (ALS DATA1) sources 0: ALS PD 1: IR PD
			INTPDSEL_ ALS2_I2C	5	1	Selection of ALS phase2 (ALS DATA2) sources 0: ALS PD 1: IR PD
			INTPDSEL_ ALS3_I2C	4	1	Selection of ALS phase3 (ALS DATA3) sources 0: ALS PD 1& ALS_DARK_EN_I2C=0: IR PD 1& ALS_DARK_EN_I2C=1: Dark PD
			RESERVE	3:2	01	RESERVE
			ALS_DARK_ EN_I2C	1	1	ALS Dark PD is selected for ALS phase3 0: Not selected 1: Selected
			RESERVE	0	1	RESERVE

Register(0x05)

Address	Type	Default	Name	BIT	Default	Description
0x05	RW	0xff	INT_WIDTH0	7:0	FF	int_width = INT_WIDTH[9:0]*(1/CK); INT_WIDTH[7:0]

Register(0x06)

Address	Type	Default	Name	BIT	Default	Description
0x06	RW	0x41	INT_CLR	7	0	Interrupt clear bit, write a toggle to clear interrupt
			INT_NUM	6:5	10	Interrupt persistence times setting 0: 1 1: 4 2: 8 3: 16
			THRES_INT	4	0	Threshold Interrupt mode enable
			THRES_H_TO_L	3	0	Threshold Interrupt status
			THRES_INT_ FLAG	2	0	Threshold Interrupt flag
			INT_WIDTH1	1:0	01	INT_WIDTH [9:8]

Register(0x07)

Address	Type	Default	Name	BIT	Default	Description
0x07	RW	0x00	ALS_RDY_ INT_FLAG	7	0	ALS Data ready interrupt flag
			ALS_PHASE3 _BYPASS	6	0	ALS Phase3 Bypass 0: Not Bypass 1: Bypass
			ALS_PHASE2 _BYPASS	5	0	ALS Phase2 Bypass 0: Not Bypass 1: Bypass
			RESERVED	4	0	RESERVED
			RESERVED	3	0	RESERVED
			ALS_DATA _INT_CLR_SEL	2	0	ALS Data Interrupt clear mode selection 0: Self-clear 1: Manually clear
			RESERVED	1	0	RESERVED
			ALS_DATA _RDY_INT_EN	0	0	ALS Data ready interrupt enable 0: Disable 1: Enable

Register(0x0F,0x10,0x11)

Address	Type	Default	Name	BIT	Default	Description
0x0F	RW	0xFF	PRF_INTER VAL [7:0]	7:0	FF	PRF CYCLE CFG; PRF CYCLE =PRF CYCLE CFG[21:0]*Tclk; Tclk=1/1.31MHz
0x10	RW	0xFF	PRF_INTER VAL [15:8]	7:0	FF	
0x11	RW	0x3F	PRF_ERR	7	0	When the PRF setting does not meet the needs, PRF_ERR turns 1 , and after soft reset turns 0.
			RESERVED	6	0	RESERVED
			PRF_INTER VAL [21:16]	5:0	3F	PRF CYCLE CFG

Register(0x12)

Address	Type	Default	Name	BIT	Default	Description
0x12	RW	0xFF	INT_MAX _THRES [7:0]	7:0	FF	Threshold Interrupt high threshold, bits [7:0]

Register(0x13)

Address	Type	Default	Name	BIT	Default	Description
0x13	RW	0xFF	INT_MAX _THRES [15:8]	7:0	FF	Threshold Interrupt high threshold, bits [15:8]

Register(0x14)

Address	Type	Default	Name	BIT	Default	Description
0x14	RW	0xFF	INT_MIN _THRES [7:0]	7:0	FF	Threshold Interrupt low threshold, bits [7:0]

Register(0x15)

Address	Type	Default	Name	BIT	Default	Description
0x15	RW	0xFF	INT_MAX _THRES [15:8]	7:0	FF	Threshold Interrupt low threshold, bits [15:8]

Register(0x16)

Address	Type	Default	Name	BIT	Default	Description
0x16	RW	0x01	RESERVED	7	0	RESERVED
			ADC GAIN SEL	6:4	000	ALS ADC gain： 0：1X 1：2X 2：4X 3：8X 4：16X 5：32X
			RESERVED	3:2	00	RESERVED
			SETUP_SEL	1:0	01	Setup time width： 0：32 1：64 2：128 3：256 Unit is Tclk

Register(0x17)

Address	Type	Default	Name	BIT	Default	Description
0x17	RW	0x08	ALS_CUAMP GAIN_SEL	7:4	0001	ALS current amplifier gain： 0：256X 1：128X 2：64X 3：32X 4：16X 5：8X 6：4X 7：2X 8：1X
			RESERVED	3	0	RESERVED
			RESERVED	2	0	RESERVED
			RESERVED	1:0	00	RESERVED

Register(0x18)

Address	Type	Default	Name	BIT	Default	Description
0x18	RW	0x02	ALS INTERVAL	7:0	02	ALS phase3 conversion interval

Register(0x19)

Address	Type	Default	Name	BIT	Default	Description
0x19	RW	0x7F	ADC INTCAPSEL	7:0	7F	ALS ADC INTCAPSEL

Register(0xC1)

Address	Type	Default	Name	BIT	Default	Description
0xC1	RW	0x85	RESERVED	7	1	RESERVED
			Current Offset	6	0	Offset enable
			RESERVED	5	0	RESERVED
			ALS self-test	4	0	ALS self-test
			RESERVED	3	0	RESERVED
			DIODESEL	2	1	0: LOW PD 1: HIGH PD
			RESERVED	1	0	RESERVED
			OPDRAINEN	0	1	INT PIN mode

Register(0xC7)

Address	Type	Default	Name	BIT	Default	Description
0xC7	RW	0x00	ADCNRZEN	7	0	ADC NRZ mode enable
			RESERVED	6	0	RESERVED
			ADCINTOPOFFEN	5	0	ADC Integtor OP offset enable
			RESERVED	4:0	0	RESERVED

Register(0xA4)

Address	Type	Default	Name	BIT	Default	Description
0xA4	RO	0x00	ALS_DATA1 [7:0]	7:0	00	ALS DATA1, bits [7:0]

Register(0xA5)

Address	Type	Default	Name	BIT	Default	Description
0xA5	RO	0x00	ALS_DATA1 [15:8]	7:0	00	ALS DATA1, bits [15:8]

Register(0xA6)

Address	Type	Default	Name	BIT	Default	Description
0xA6	RO	0x00	ALS_DATA2 [7:0]	7:0	00	ALS DATA2, bits [7:0]

Register(0xA7)

Address	Type	Default	Name	BIT	Default	Description
0xA7	RO	0x00	ALS_DATA2 [15:8]	7:0	00	ALS DATA2, bits [15:8]

Gain configuration

ALS Loop Gain	ADC gain	ALS current amplifier gain	Register(0x16)	Register(0x17)
2048X	8X	256X	0x33	0x08
1024X	4X	256X	0x23	0x08
256X	2X	128X	0x13	0x18
64X	1X	64X	0x03	0x28
16X	1X	16X	0x03	0x48
4X	1X	4X	0x03	0x68
1X	1X	1X	0x03	0x88

Integration time

Single phase ALS Integrate time = 2^ ALS_ADC_OSR * TCLK (TCLK=(1/1.31MHz)

ALS_ADC_OSR	0x01 bit[6:4]	Integral time(single channel)
16	100	50ms
15	011	25ms
14	010	12.5ms
13	001	6.25ms
12	000	3ms

I2C Protocol

I2C Data format

The I2C bus protocol was developed by Philips (now NXP). The device supports the standard writing and reading protocol. The 7-bit device address is 0x44. The register index will automatically increase by 1 after the addressed register has been accessed (read or write). And the format is shown as following:

A Acknowledge (0)

N Not Acknowledge (1)

P Stop Condition

R Read (1)

S Start Condition

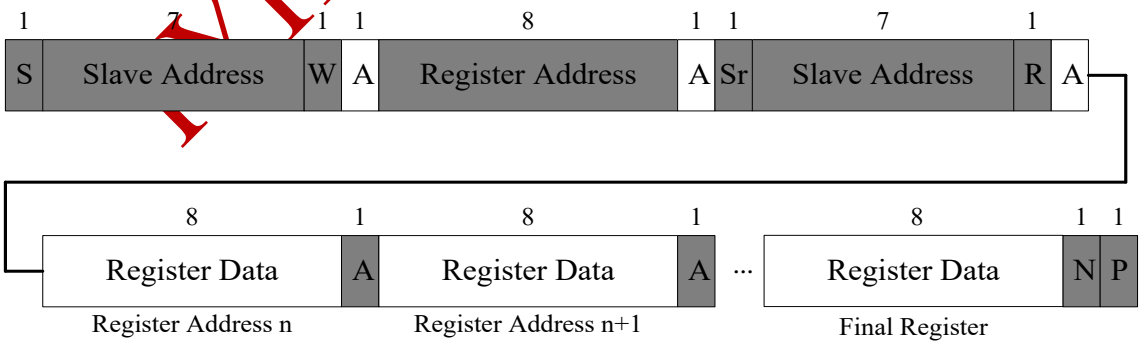
W Write (0)

Sr Repeated Start Condition

■Master-to- Slave

□ Slave-to-Master

I2C Write Register Data



I2C Read Register Data

Figure7 I²C Write/Read operation

I2C Electrical Characteristics

Table1 Electrical Characteristics

PARAMETER	SYMBOL	STANDARD-MODE		FAST-MODE		UNIT
		MIN	MAX	MIN	MAX	
LOW level input voltage: fixed input levels (Vbus=1.8V) VDD-related input levels (Vbus=LEDA)	VIL	 0.5	 0.54 0.3Vbus	 n/a 0.5	 n/a 0.3Vbus(1)	 V V
HIGH level input voltage: fixed input levels (Vbus=1.8V) VDD-related input levels (Vbus=LEDA)	VIH	 1.26 0.7Vbus	 n/a Note(2)	 1.26 0.7Vbus(1)	 n/a Note(2)	 V V
Hysteresis of Schmitt trigger inputs: Vbus > 2 V Vbus < 2 V	Vhys	 n/a n/a	 n/a n/a	 0.05Vbus 0.1Vbus	 – –	 V V
LOW level output voltage (open drain or open collector) at 3 mA sink current: Vbus > 2 V Vbus < 2 V	 VOL1 VOL2	 0 n/a	 0.4 n/a	 0 0	 0.4 0.2Vbus	 V V
Output fall time from VIHmin to VILmax with a bus capacitance from 10 pF to 400 pF	tof	–	250(4)	20+0.1 Cb(3)	250(4)	ns
Pulse width of spikes which must be suppressed by the input filter	tSP	n/a	n/a	0	50	ns
Input current each I/O pin with an input voltage between 0.1VDD and 0.9VDDmax	Ii	-10	10	-10(5)	10(5)	A
Capacitance for each I/O pin	Ci	-	10	-	10	pF

Notes

1. Devices that use non-standard supply voltage switch don't conform to the intended I2C-bus system levels must relate input levels to the VDD voltage to which the pull-up resistors Rp are connected.
2. Maximum $V_{IH} = V_{DDmax} + 0.5V$.
3. C_b = capacitance of one bus line in pF.
4. The maximum t_f for the SDA and SCL bus lines quoted in Table1 (300ns) is longer than the specified maximum t_{of} for the output stages (250 ns). This allows series protection resistors (R_S) to be connected between the SDA/SCL pins and the SDA/SCL bus lines without exceeding the maximum specified tf.
5. I/O pins of Fast-mode devices must not obstruct the SDA and SCL lines if VDD is switched off.

n/a = not applicable

I2C Timing

The I2C Timing is as following figure:

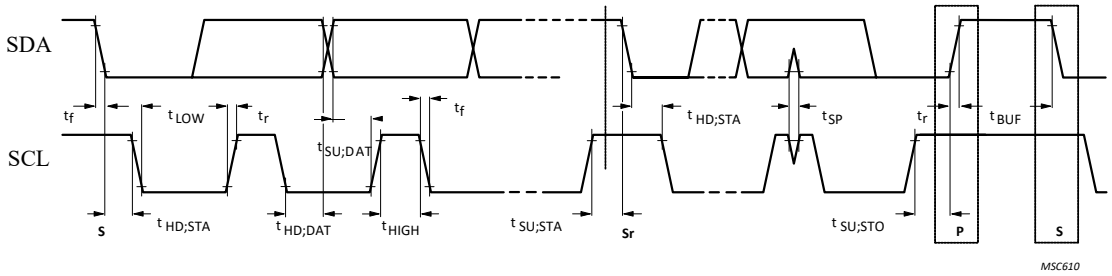


Figure8 I²C Timing

Table2 I²C Timing Parameters(1)

PARAMETER	SYMBOL	STANDARD-MODE		FAST-MODE		UNIT
		MIN	MAX	MIN	MAX	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	4.0	–	0.6	–	us
LOW period of the SCL clock	t_{LOW}	4.7	–	1.3	–	us
HIGH period of the SCL clock	t_{HIGH}	4.0	–	0.6	–	us
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	–	0.6	–	us
Data hold time	$t_{HD;DAT}$	0(2)	3.45(3)	0(2)	0.9(3)	us
Data set-up time	$t_{SU;DAT}$	250	–	100(4)	–	ns
Rise time of both SDA and SCL signals	tr	–	1000	20+0.1Cb(5)	300	ns
Fall time of both SDA and SCL signals	tf	–	300	20+0.1Cb(5)	300	ns
Set-up time for STOP condition	$t_{SU;STO}$	4.0	–	0.6	–	us
Bus free time between a STOP and START condition	t_{BUF}	4.7	–	1.3	–	us
Capacitive load for each bus line	Cb	–	400	–	400	pF

Notes

1. All values referred to V_{IHmin} and V_{ILmax} levels (see Table1).
2. A device must internally provide a hold time of at least 300ns for the SDA signal(referred to the VIHmin of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
4. A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement tSU;DAT⩾250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line tr max + tSU;DAT = 1000 + 250 = 1250 ns (according to the Standard-mode I2C-bus specification) before the SCL line is released.
5. Cb=total capacitance of one bus line in pF. If mixed with Hs-mode devices, faster fall-times according to Table2 are allowed.

Note： n/a = not applicable

Application Information

A typical application for HX3229-39B is shown in following Figure. The I²C signals and the Interrupt are open-drain outputs and require pull-up resistor. It is recommended use 10kΩ resistor to pull-up.

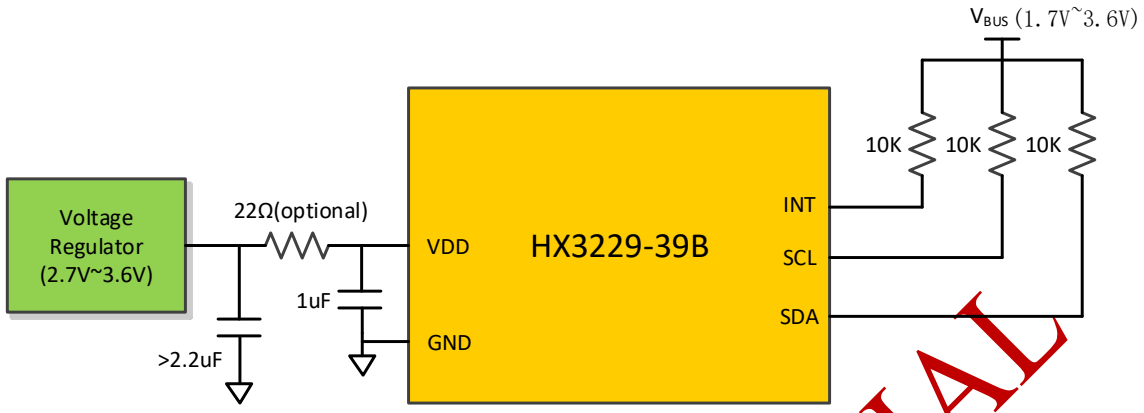
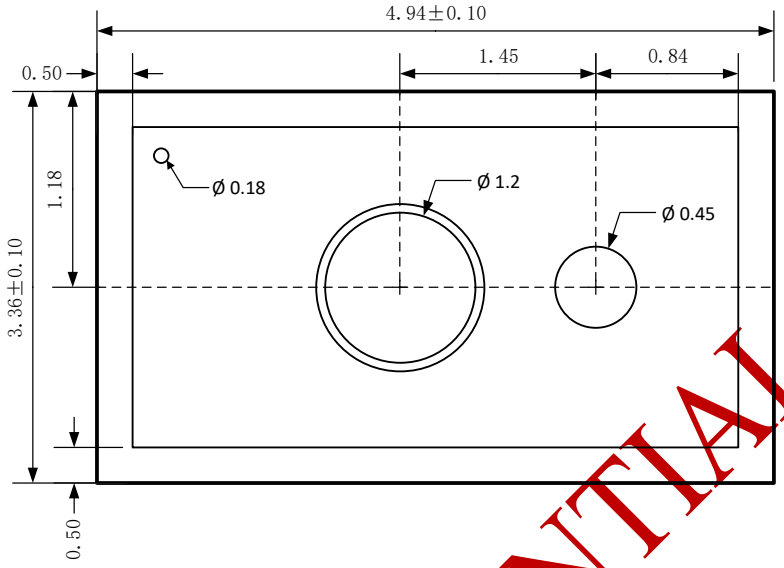


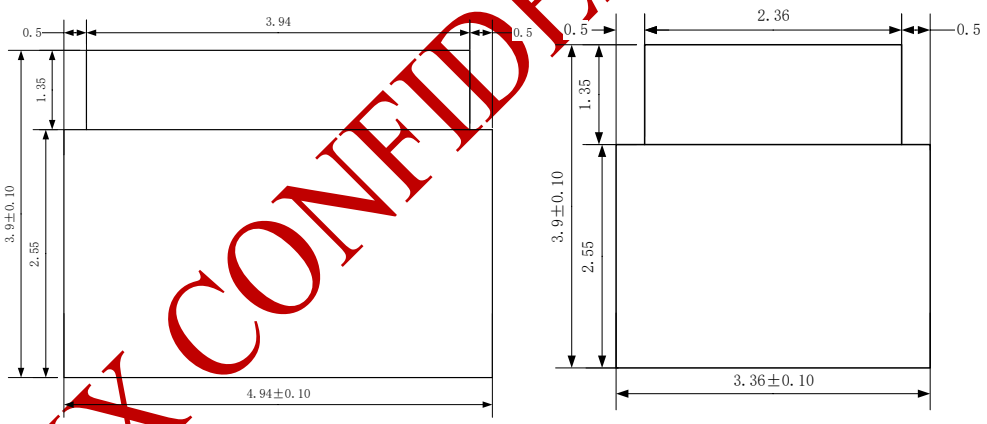
Figure9 HX3229-39B Typical Application Circuit

Package information

Top View



Side View



Bottom View

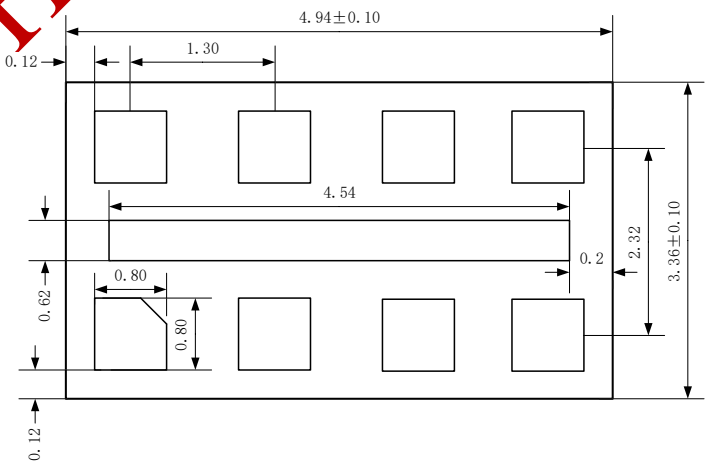


Figure10 HX3229-39B Package Information

Notes:

All linear dimensions are in mm. Dimension tolerance is ±0.05mm unless otherwise noted.

Recommended PCB Pad Layout

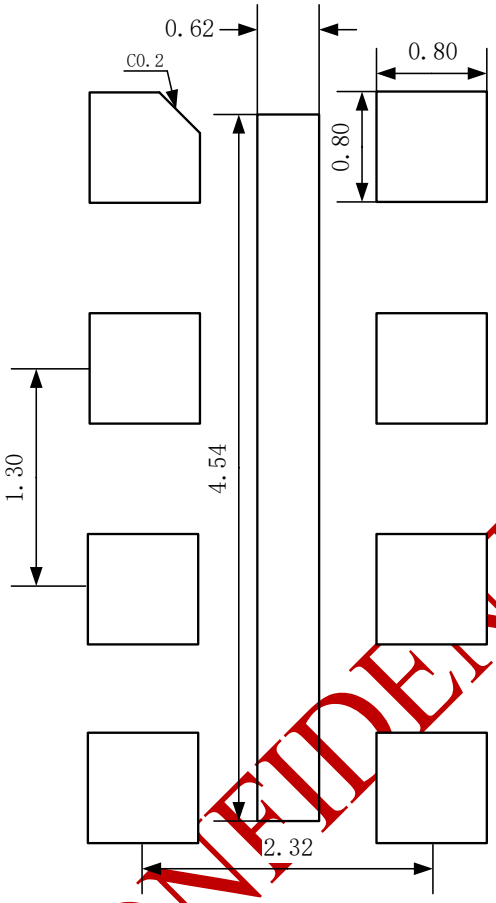


Figure11 HX3229-39B PCB Pad Layout Size

Notes:

All linear dimensions are in mm. Dimension tolerance is ±0.05mm unless otherwise noted.

Soldering Information

The module has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate, the process, equipment material used in these test are detailed below, the solder reflow profile describes the expect maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

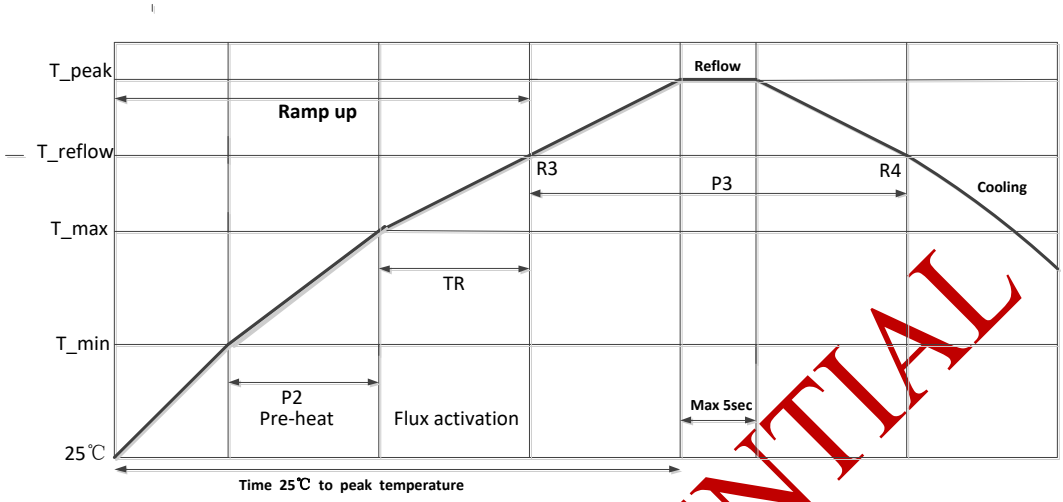


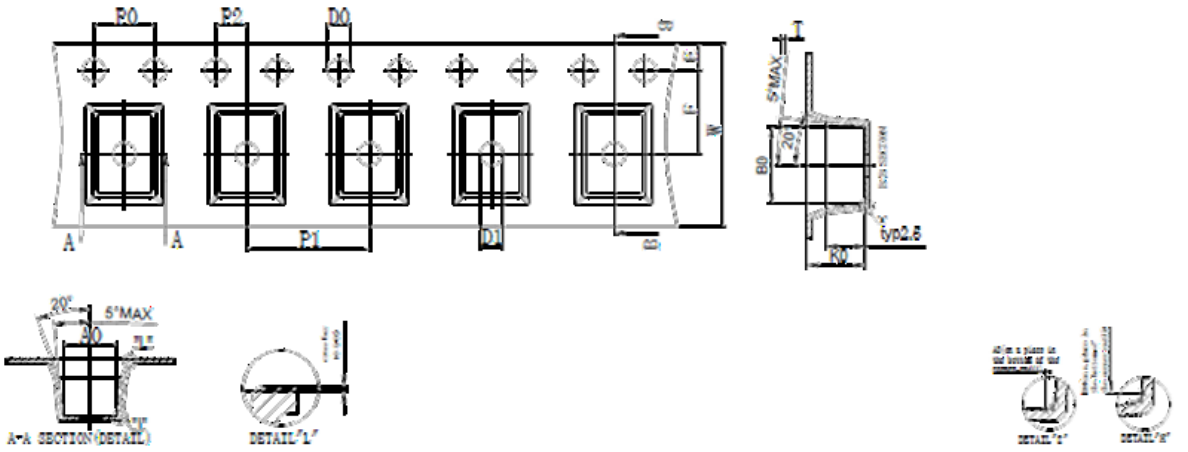
Figure12 HX3229-39B Reflow Profile Graph

The detail parameter is as following table:

Table3 Solder Reflow Profile

	Peak temperature (Tpeak)	250℃; Max 5sec
Pre-Heat	Temperature min (Tmin)	150℃; 2℃/Sec
	Temperature max(Tmax)	150-217℃； 100S to 180S
	P2：（T min to max）	90-110s
Time maintain above	Temperature (Treflow)	217 ℃
	Time (P3)	60-90sec
	R3 Slope (from 217℃to peak)	2℃/sec(typ) to 2.5℃/sec(max)
	R4 Slope (from peak to 217℃)	1.5℃/sec(typ) to 4℃/sec(max)
	Time to peak temperature	480s Max
	Cooling down slope (peak to 217℃)	2-4℃/sec

Carrier Drawing



ITEM	A0	B0	K0	P0	P1	P2	T	E	F	D0	D1
Spec	3.60±0.10	3.20±0.10	1.00±0.10	4.00±0.10	8.00±0.10	2.00±0.10	0.30±0.05	1.75±0.10	3.50±0.10	1.50$^{+0.10}_{0}$	1.0MIN
ITEM	W	10P0									
Spec	12.00±0.30	40.00±0.20									

Figure13 HX3229-39B Packing Information

The Maximum capacity of one packing box:One Inner packing box = 1000PCS

Note:The Tape and Reel packing with vacuum pack is 1 year storage available @25℃， 50%RH。

REVISION HISTORY

Version	Date	Comment
1.0	Aug 21, 2021	Initial version
1.1	Aug 04, 2022	