Ambient Light And Proximity Sensor Module

HX32062S

Features

Ambient Light Sensor

1.Up to 24 bits ADC for high resolution ALS.
2.Ultra-high sensitivity and ultra-low noise to remove additional dedicated ALS sensor.
3. Wide range, flexible and high linear gain control: 1X/2x/……/1024x.
4. FOV up to 100 deg for better performance in dark environment.
5. Excellent spectral response similar to human-eye response and suppress IR portion.
6. Flexible interrupt setting.
7. Low power consumption:150uA with a single channel on.
8. Smart on-chip calibration for easy manufacture.

Proximity Sensor

1. Excellent ambient light suppression.
2. Wide range analog cross-talk cancellation.
3. Configurable proximity detection resolution, up to 16 bits.
4.Flexible interrupt setting with configurable persistence setting
5. Low power consumption without IR LED operation:200uA.
6. Smart on-chip calibration for easy manufacture.
7. Build-in 940nm IR LED

General

1. power supply with VDD operation voltage: 1.7V~2.0 V
2. IR power supply with VDD3 operation voltage: 2.7V~3.6 V
3. I^2C interface, 1.7V~3.6V.
4. Compact Size: 4.0mm x 1.5mm x1 mm OLGA8

Applications

Smart Phone, PAD, TWS
Head Phone, Smart Wearable

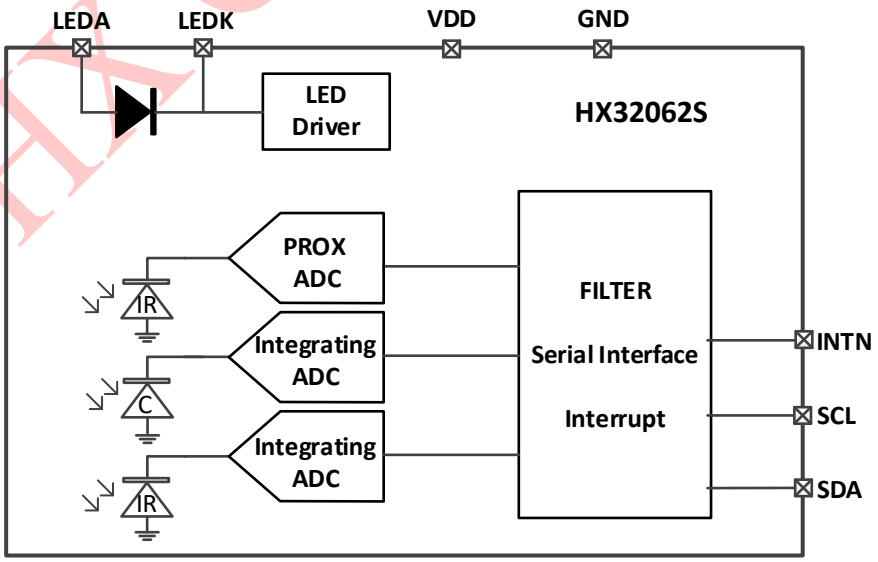
Description

HX32062S is an optical sensor with a built-in IR LED and I2C interface. With excellent ambient light detection capability, the device provides ambient light sensing judgment to realize backlight and display brightness control, and at the same time, it senses infrared light to realize judgment for proximity and distance.

Ambient light sensor (ALS) utilizes photo-diode with spectral similar to the human eye response. The amplified photo-diode current is converted to an integrated ADC with adjustable resolution to detect a wide range of light intensity environment. The typical integrate time is set as 100ms which can reject the 50Hz/60Hz flickering noise caused by indoor light source.

The proximity sensing is realized by using LED, a proximity detection photo-diode, IR LED driver circuit, as well as proximity detection algorithm. There is various wait time and sleep modes programmed through I2C interface to provide low power operation.

Simplified Block Diagram



Contents

1 Pin Configuration

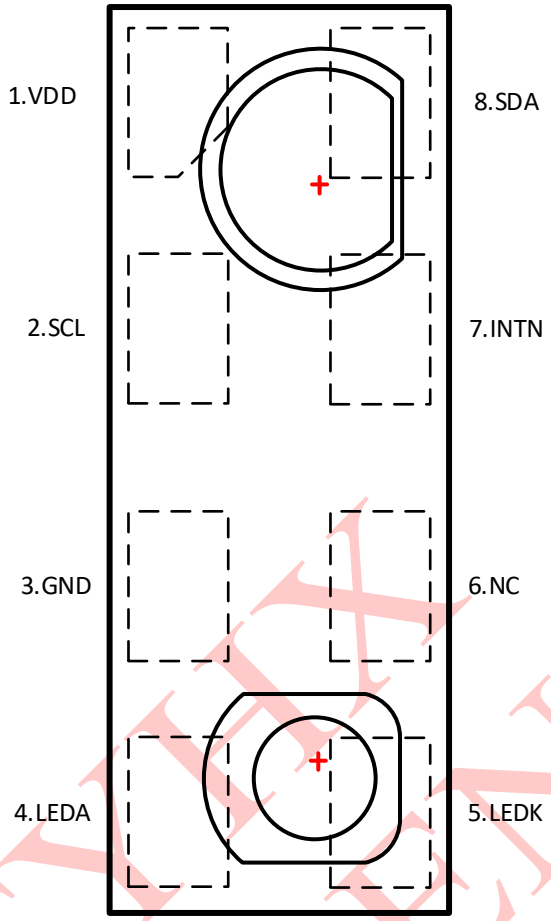


Figure1 HX32062S Pin Diagram

Table1 HX32062S Pin Description

Pin	Name	Type	Description
1	VDD	PWR	Power supply: 1.7V to 2.0V
2	SCL	I2C	I2C CLK, external pull up resistor
3	GND	GND	Power Ground
4	LEDA	PWR	Anode of the embedded IR LED, connect to power
5	LEDK	IN	IR LED driver pin connecting to the cathode of the external IR LED
6	NC		No Connect
7	INTN	DIG IN	Interrupt pin
8	SDA	I2C	I2C data, external pull up resistor

2 Specifications

2.1 Absolute Maximum Rating

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VDD	-0.3		2.0	V
IR Emitter Voltage to GND	VDD3	-0.5		3.6	V
Storage temperature	Tstg	-40		85	℃

2.2 Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	VDD	1.7	1.8	2.0	V
Voltage of LED's anode	VLEDA	2.8	3.3	3.6	V
Operation temperature, functional	Ta	-30		85	℃
Operation temperature, best performance		-20		65	℃
Clock frequency of I2C	F_{I2C}			400	KHz
HBM	ESD			2	KV

2.3 Electrical Characteristics

Typical specifications are at 25°C, VDD=1.8V, VDD3=3.3V .

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
General characteristics					
Power Consumption		150		uA	ALS only Single channel
		300		uA	ALS only Double channel
		100		uA	PS only LED current excluded
		1.2		uA	Power down
ALS characteristics					
ALS Range	0		100K	Lux	Gain=1X White LED is used
ALS Dark offset			2	Count	No Input Light
ALS Resolution		0.3		mLux	
ALS Gain	1		1024		
ADC Resolution		24		Bits	
FOV		100		degree	
PS characteristics					
LED Wavelength		940		nm	
ADC Resolution		16		Bits	
CLK					
Frequency		20		MHz	
I2C INTERFACE					
Maximum Clock Speed		400		KHz	

3 Detailed Description

3.1 Overview

HX32062S is an optical sensor with integrated digital ambient light sensor (ALS), digital proximity sensor (PS), 940nm IR LED and driver in a single 8-pin package. This device provides a very high sensitivity ambient light sensing within visible spectral range and infrared sensing for proximity measurement.

For ambient light sensing, HX32062S includes a photo-diode, digital state machine, wide range gain control and very low noise ADC in a single chip. The excellent spectral response is designed to be close to human eye. With 1x to 1024x gain, HX32062S is suitable for detecting a wide range of light intensity environment.

For proximity sensing, HX32062S also includes a photo-diode, digital state machine, IR LED, LED driver and high-resolution ADC in the same package. HX32062S employs an analog digital mixed noise cancellation scheme to highly reject unwanted ambient noise.

HX32062S has excellent temperature compensation, analog crosstalk light cancellation and calibrated on-chip oscillator. Software shutdown mode control is provided for low power application. HX32062S operating voltage range is 1.7V to 2.0V.

3.2 Functional Block Diagram

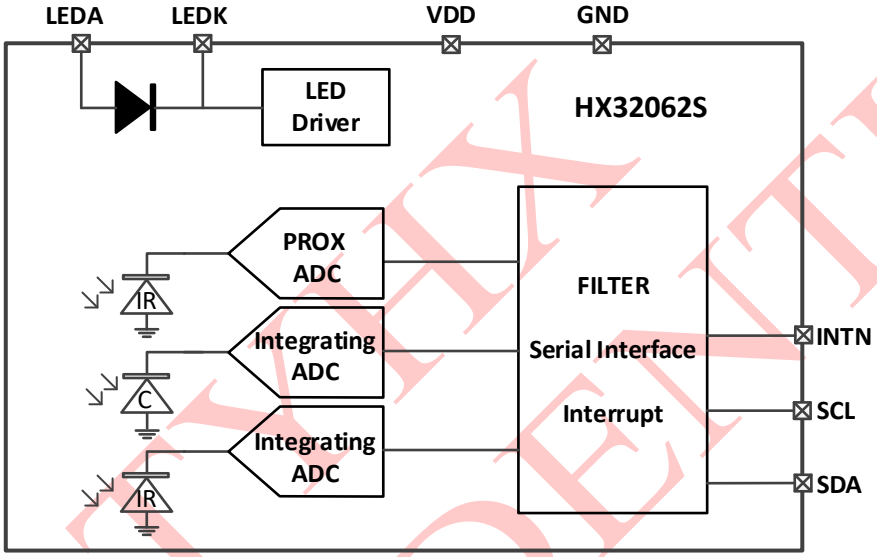


Figure2 Functional Block Diagram

3.3 ALS curve in typical configuration

Typical specifications are at 25°C. VDD=1.8V, VDD3=3.3V Gain=1024X, ALS 24 bits resolution. The ALS curve of the HX32062S is shown in the following figure, with white LED.

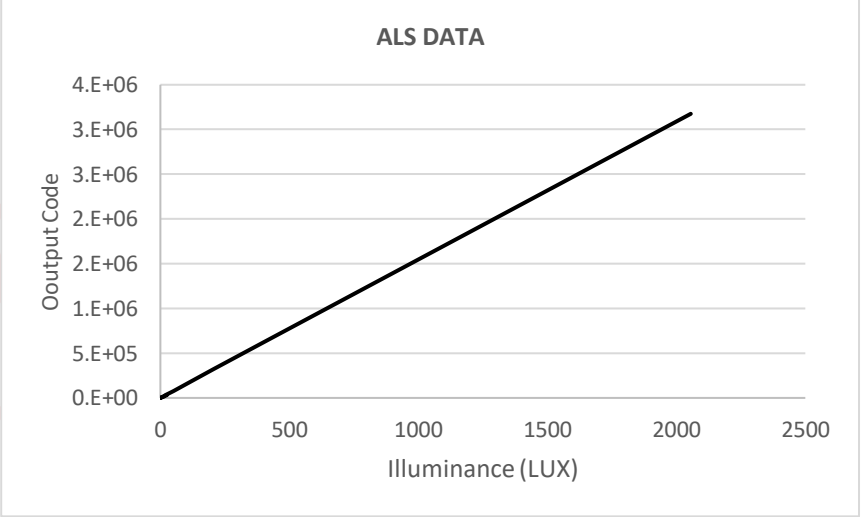


Figure3 Typical ALS curve

3.4 ALS angular response

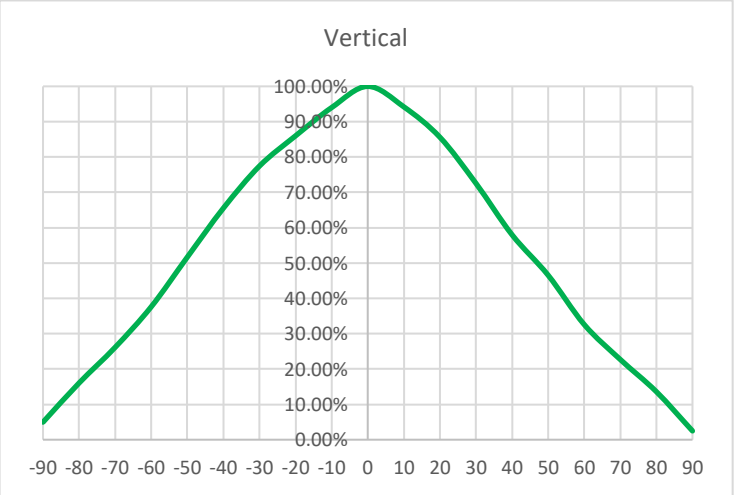


Figure4 ALS FOV

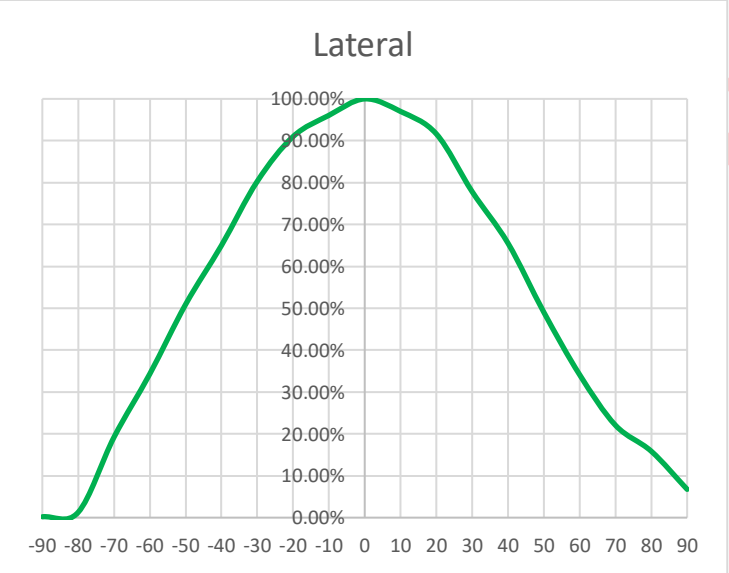


Figure5 ALS FOV

3.5 ALS response curve

The PD corresponding to the ALS was coated, and the PD response curve after coating was as shown.

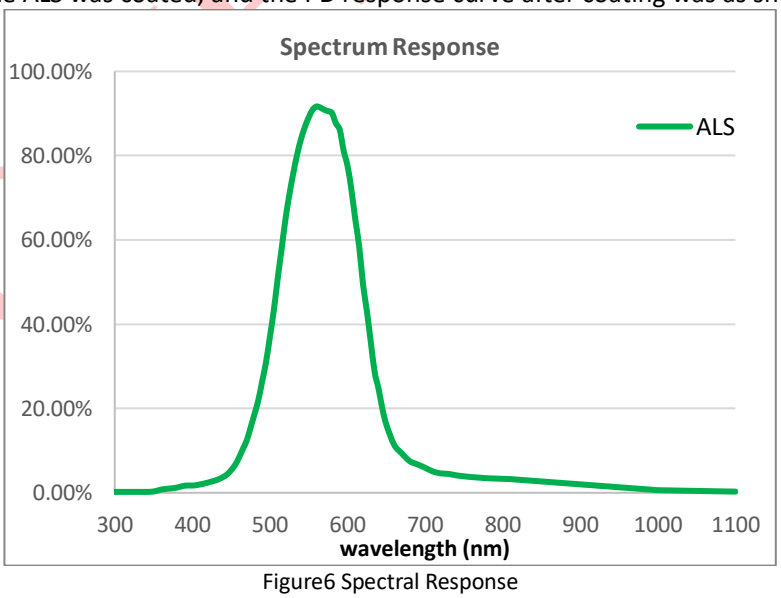


Figure6 Spectral Response

3.6 Gray card distance and PS value

Figure7 PS value and gray card distance curve

3.7 PS response curve

The PD response curve after coating is as shown.

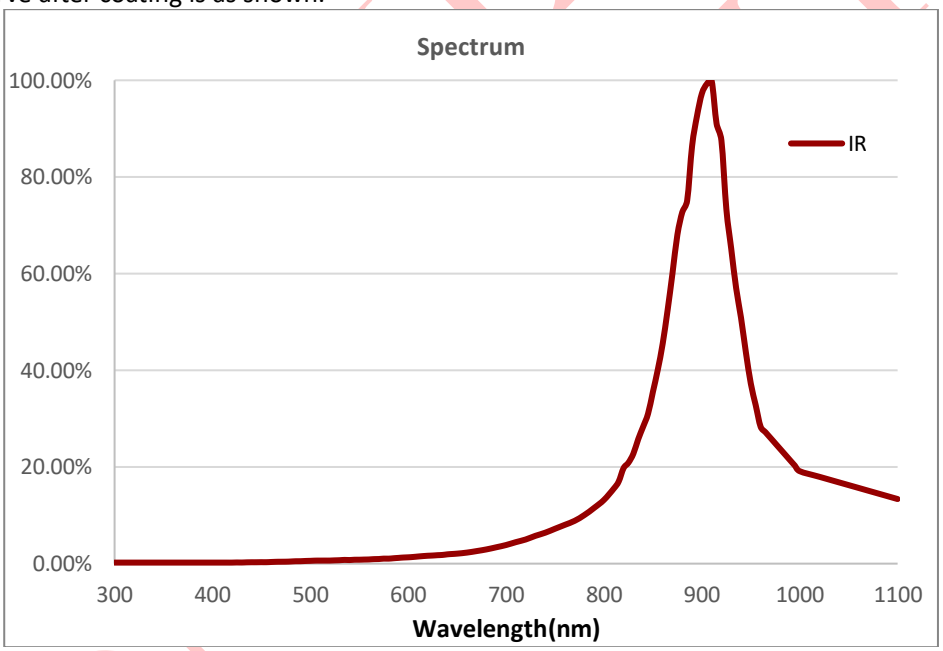


Figure8 PS PD Spectral Response

4 Register Map

Address	Name	R/W	BIT	Function	Default
0x00	RA_DEVICE_ID	RO	<7:0>	DEVICE_ID	0x32
0x01	RA_ALS1_LP_DATA0	RO	<7:0>	ALS1_RAW_DATA	0x00
0x02	RA_ALS1_LP_DATA1	RO	<7:0>		0x00
0x03	RA_ALS1_LP_DATA2	RO	<7:0>		0x00
0x04	RA_ALS2_LP_DATA0	RO	<7:0>	ALS2_RAW_DATA	0x00
0x05	RA_ALS2_LP_DATA1	RO	<7:0>		0x00
0x06	RA_ALS2_LP_DATA2	RO	<7:0>		0x00
0x07	RA_ALS3_LP_DATA0	RO	<7:0>	ALS3_RAW_DATA	0x00
0x08	RA_ALS3_LP_DATA1	RO	<7:0>		0x00
0x09	RA_ALS3_LP_DATA2	RO	<7:0>		0x00
0x0A	RA_ALS4_LP_DATA0	RO	<7:0>	ALS4_RAW_DATA	0x00
0x0B	RA_ALS4_LP_DATA1	RO	<7:0>		0x00
0x0C	RA_ALS4_LP_DATA2	RO	<7:0>		0x00
0x0D	RA_PS_RAW_DATA0	RO	<7:0>	PS_RAW_DATA	0x00
0x0E	RA_PS_RAW_DATA1	RO	<7:0>		0x00
0x0F	RA_PS_RAW_DATA2	RO	<7:0>		0x00
0x10	RA_PS_BL_DATA0	RO	<7:0>	PS_BL_DATA	0x00
0x11	RA_PS_BL_DATA1	RO	<7:0>		0x00
0x12	RA_PS_BL_DATA2	RO	<7:0>		0x00
0x7A	RA_PS_DIFF_DATA0	RO	<7:0>	PS_PROX_DATA	0x00
0x7B	RA_PS_DIFF_DATA1	RO	<7:0>		0x00
0x7C	RA_PS_TEMP_OFFSET_DATA0	RO	<7:0>	PS_TEMP_OFFSET	0x00
0x7D	RA_PS_TEMP_OFFSET_DATA1	RO	<7:0>		0x00
0x7E	RA_PS_TEMP_OFFSET_DATA2	RO	<0>		0x00
0x13	RA_DATA_RDY_CTRL0	RW	<5>	Als2 the threshold interrupt function is enabled	0x30
			<4>	Als1 the threshold interrupt function is enabled	
			<3>	Als4 ready interrupt enable	
			<2>	Als3 ready interrupt enable	
			<1>	Als2 ready interrupt enable	
			<0>	Als1 ready interrupt enable	
0x14	RA_DATA_RDY_CTRL1	RW	<4>	Interrupt mark read clear enable	0x02
			<1>	PS level 1 threshold interrupt is enabled	
			<0>	PS ready interrupt enable	
0x15	RA_DATA_RDY_FLAG0	RO	<3>	Als4 ready interrupt flag	0x00
			<2>	Als3 ready interrupt flag	
			<1>	Als2 ready interrupt flag	
			<0>	Als1 ready interrupt flag	
0x16	RA_DATA_RDY_FLAG1	RO	<5>	Als2 low threshold interrupt flag	0x00
			<4>	Als1 low threshold interrupt flag	
			<1>	Als2 high threshold interrupt flag	
			<0>	Als1 high threshold interrupt flag	
0x17	RA_DATA_RDY_FLAG2	RO	<0>	PS ready interrupt flag	0x00
0x18	RA_DATA_RDY_FLAG3	RO	<3>	PS second level low threshold interrupt flag	0x00
			<2>	PS second level high threshold interrupt flag	
			<1>	PS first level low threshold interrupt flag	
			<0>	PS first level high threshold interrupt flag	
0x19	RA_ALS_DIV_CLK_CTRL	RW	<7:4>	ALS2 sampling clock frequency 0:1.6MHz 1:800KHz 2:400KHz 3:200KHz 4:100KHz 5:50KHz 6:25KHz 7:12.5KHz 8:6.25KHz	0x44

			<3:0>	ALS1 sampling clock frequency 0:1.6MHz 1:800KHz 2:400KHz 3:200KHz 4:100KHz 5:50KHz 6:25KHz 7:12.5KHz 8:6.25KHz	
0x1A	RA_GLOBAL_CTRL0	RW	<2>	Soft reset	0x05
0x20	RA_ALS1_CTRL0	RW	<6:4>	ALS1 AVG NUM: 0: 1 1: 2 2: 4 3: 8 4: 16 5: 32 6: 64	0x30
			<2:1>	ALS1 An interruption occurs when the threshold is reached for N consecutive times： 0: 1 1: 2 2: 4 3: 8	
			<0>	ALS1 continue enable signal	
0x21	RA_ALS1_CTRL1	RW	<6:4>	ALS1 OSR NUM: 0: 32 1: 64 2: 128 3: 256 4: 512 .default	0x45
0x23	RA_ALS1_CTRL3	RW	<5:4>	ALS LP FILTER 0: 1 1:1/2 2:1/4 3:1/8 default:0	0x00
			<2:0>	ALS1 number of interval ODRs Run once： 0: 1 1: 2 2: 4 3: 8 4: 16 5: 32 6: 64 7：128	
0x24	RA_ALS1_CTRL4	RW	<0>	ALS1 enable signal	0x00
0x25	RA_ALS1_THR_INT_HIGH0	RW	<7:0>	ALS1 high threshold Interrupt value	0x00
0x26	RA_ALS1_THR_INT_HIGH1	RW	<7:0>	ALS1 high threshold Interrupt value	0xc0
0x27	RA_ALS1_THR_INT_LOW0	RW	<7:0>	ALS1 low threshold Interrupt value	0x00
0x28	RA_ALS1_THR_INT_LOW1	RW	<7:0>	ALS1 low threshold Interrupt value	0x40
0x29	RA_ALS1_GAIN_CFG	RW	<3:0>	ALS1 Analog Gain 0001: Gain = 1X 0010: Gain = 2X 0011: Gain = 4X 0100: Gain = 8X 0101: Gain = 16X 0110: Gain = 32X	0x06
0x2A	RA_ALS1_AFE_OFFSET0	RW	<7:0>	ALS1 AFE OFFSET DATA	0x00
0x2B	RA_ALS1_AFE_OFFSET1	RW	<7:0>		0x00
0x2C	RA_ALS1_AFE_OFFSET2	RW	<7:0>		0x00
0x2D	RA_ALS1_AFE_OFFSET3	RW	<0>		0x00
0x30	RA_ALS2_CTRL0	RW	<6:4>	ALS2 AVG NUM: 0: 1 1: 2 2: 4	0x30

				3: 8 4: 16 5: 32 6: 64	
			<0>	ALS2 continue enable signal	
0x31	RA_ALS2_CTRL1	RW	<6:4>	ALS2 OSR NUM: 0: 32 1: 64 2: 128 3: 256 4: 512	0x45
0x33	RA_ALS2_CTRL3	RW	<2:0>	ALS2 ODR NUM： 0: 1 1: 2 2: 4 3: 8 4: 16 5: 32 6: 64 7：128	0x00
0x34	RA_ALS2_CTRL4	RW	<0>	ALS2 enable signal	0x00
0x39	RA_ALS2_GAIN_CFG	RW	<3:0>	ALS2 Analog Gain 0001: Gain = 1X 0010: Gain = 2X 0011: Gain = 4X 0100: Gain = 8X 0101: Gain = 16X 0110: Gain = 32X	0x06
0x3A	RA_ALS2_AFE_OFFSET0	RW	<7:0>	ALS2 AFE OFFSET DATA	0x00
0x3B	RA_ALS2_AFE_OFFSET1	RW	<7:0>		0x00
0x3C	RA_ALS2_AFE_OFFSET2	RW	<7:0>		0x00
0x3D	RA_ALS2_AFE_OFFSET3	RW	<0>		0x00
0x4A	RA_ALS3_GAIN_CFG	RW	<3:0>	ALS3 Analog Gain 0001: Gain = 1X 0010: Gain = 2X 0011: Gain = 4X 0100: Gain = 8X 0101: Gain = 16X 0110: Gain = 32X	0x06
0x4B	RA_ALS4_GAIN_CFG	RW	<3:0>	"ALS4 Analog Gain 0001: Gain = 1X 0010: Gain = 2X 0011: Gain = 4X 0100: Gain = 8X 0101: Gain = 16X 0110: Gain = 32X"	0x06
0x53	RA_PS_CTRL3	RW	<7:2>	PS LED pulse width: 2us+N*1us, default 64us	0xf4
0x5A	RA_PS_GAIN_CFG0	RW	<3:0>	Analog Multi-Sample:1/2/4/8/16/32/64/128/256	0x02
0x5B	RA_PS_GAIN_CFG1	RW	<3:0>	Digital-MultiSample the number can match: 1/2/4/8/16/32/64/128/256	0x01
0x60	RA_PS_FRIST_TIME_THRES0	RW	<7:0>		0x1000
0x61	RA_PS_FRIST_TIME_THRES1	RW	<7:0>		
0x62	RA_PS_THR_INT_NUM	RW	RW	Proximity and distance judgment interrupt times 0: 1 1: 2 2: 4 3: 8	0x0
0x64	RA_PROX_THR_HIGH1_0	RW	<7:0>	H03E8	0x03e8
0x65	RA_PROX_THR_HIGH1_1	RW	<7:0>		
0x66	RA_PROX_THR_LOW1_0	RW	<7:0>	H0168	0x0168
0x67	RA_PROX_THR_LOW1_1	RW	<7:0>		
0x6C	RA_PS_OFFSET_0	RW	<7:0>		0x00

0x6D	RA_PS_OFFSET_1	RW	<7:0>		
0x6E	RA_PS_OFFSET_2	RW	<0>		0x00
0x6F	RA_PS_UP_THRES	RW	<7:0>	PS_RAW_DATA[N] < PS_BL_DATA[N-1]+PS_UP_THRES<7:0>	0x00
0x70	RA_PS_BL_DATA_LOW_THRES	RW	<7:0>	PS_BL_DATA_LOW_THRES<7:0>,9d0	0x80
0x80	RA_ODR_CFG0	RW	<4:0>	" 00000: Min (no idle time) 00001: 0.4 ms =d640; 00010: 0.6 ms =d960; 00011: 0.8ms =d1280; 00100: 1 ms =d1600; 00101: 2 ms =d3200; 00110: 4 ms =d6400; 00111: 6 ms =d9600; 01000: 8 ms =d12800; 01001: 10 ms =d16000; 01010: 12 ms =d19200; 01011: 14 ms =d22400; 01100: 16 ms =d25600; 01101: 20 ms =d32000; 01110: 25 ms =d40000; 01111: 30 ms =d48000; 10000: 40 ms =d64000; 10001: 50 ms =d80000; 10010: 60 ms =d96000; 10011: 75 ms =d120000; 10100: 80 ms =d128000 10101: 90 ms =d144000; 10110: 100 ms(Typ)=d160000; 10111: 200 ms =d320000; 11000: 300 ms =d480000; 11001: 400 ms =d640000; 11010: 800 ms =d1280000; 11011: 1s =d1600000 11100: 1.6 s = d2560000 11101: 2 s =d3200000; 11110: 3 s =d4800000; 11111: 4 s =d6400000;"	0x16
0x83	RA_DATA_LOCK_CFG	RW	<6>	Interrupt Type selection 0=pulse 1=level	0x01
			<5>	Manually clear interrupts and flag	
			<4>	LOCK eliminate	
			<3>	Interrupt clear mode	
			<2>	Timeout enabled	
			<1>	Manual LOCK	
			<0>	Read LOCK enabled	
0x84	RA_TIMEOUT_CFG0	RW	<7:0>	timeout_num[7:0]	
			<7:0>		
0x86	RA_TIMEOUT_CTRL_FLAG	RW	<1>	timeout flag	
			<0>	Timeout interrupt enable signal	
0x87	RA_INT_WIDTH_CFG0	RW	<7:0>	int_width_num[14:0], unit 625ns， default 1ms	0x0640
0x88	RA_INT_WIDTH_CFG1	RW	<7:0>		
0xe3	RA_LED_CURRENT_CFG	RW	<6:3>	LED current, unit 1mA, default 15mA	0x7F

5 I2C Protocol

5.1 I2C Data format

The I2C bus protocol was developed by Philips (now NXP). The device supports the standard writing and reading protocol. The 7-bit device address is 0x2B. The register index will automatically increase by 1 after the addressed register has been accessed (read or write). And the format is shown as following:

A Acknowledge (0)

P Stop Condition

R Read (1)

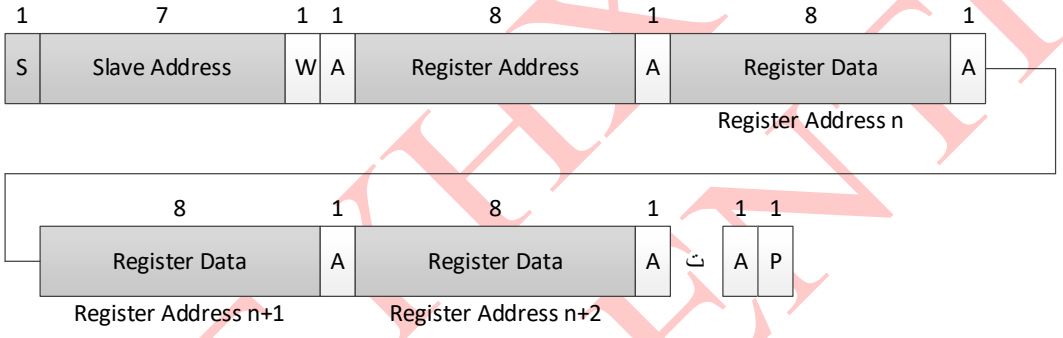
S Start Condition

W Write (0)

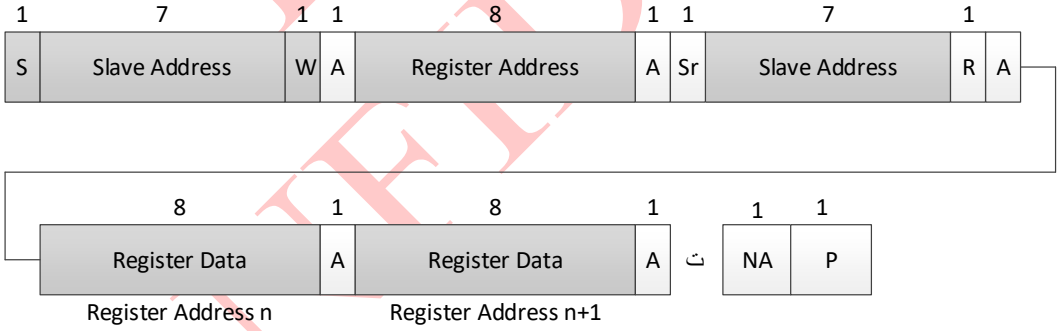
Sr Repeated Start Condition

■Master-to- Slave

□ Slave-to-Master



I2C Write Register Data



I2C Read Register Data

Figure9 I2C data format diagram

5.2 I2C Electrical Characteristics

Table2 I²C Electrical Characteristics

PARAMETER	SYMBOL	STANDARD-MODE		FAST-MODE		UNIT
		MIN	MAX	MIN	MAX	
LOW level input voltage: fixed input levels VDD-related input levels	VIL	 0.5 0.5	 1.5 0.3VDD	 n/a 0.5	 n/a 0.3VDD(1)	 V V
HIGH level input voltage: fixed input levels VDD-related input levels	VIH	 3 0.7VDD	 Note(2) Note(2)	 3 0.7VDD(1)	 n/a Note(2)	 V V
Hysteresis of Schmitt trigger inputs: VDD > 2 V	Vhys	 n/a	 n/a	 0.05VDD	 –	 V

VDD < 2 V		n/a	n/a	0.1VDD	–	V
LOW level output voltage (open drain or open collector) at 3 mA sink current: VDD > 2 V VDD < 2 V	 VOL1 VOL2	 0 n/a	 0.4 n/a	 0 0	 0.4 0.2VDD	 V V
Output fall time from VIHmin to VILmax with a bus capacitance from 10 pF to 400 pF	tof	–	250(4)	20+0.1 Cb(3)	250(4)	ns
Pulse width of spikes which must be suppressed by the input filter	tSP	n/a	n/a	0	50	ns
Input current each I/O pin with an input voltage between 0.1VDD and 0.9VDDmax	Ii	-10	10	-10(5)	10(5)	A
Capacitance for each I/O pin	Ci	-	10	-	10	pF

Notes

1. Devices that use non-standard supply voltage switch don't conform to the intended I2C-bus system levels must relate input levels to the VDD voltage to which the pull-up resistors Rp are connected.
2. Maximum $V_{IH} = V_{DDmax} + 0.5V$.
3. C_b = capacitance of one bus line in pF.
4. The maximum t_f for the SDA and SCL bus lines quoted in Table10.3.1(300ns) is longer than the specified maximum t_{of} for the output stages (250 ns). This allows series protection resistors (R_S) to be connected between the SDA/SCL pins and the SDA/SCL bus lines without exceeding the maximum specified tf.
5. I/O pins of Fast-mode devices must not obstruct the SDA and SCL lines if VDD is switched off.

n/a = not applicable

5.3 I2C Timing

The I2C Timing is as following figure:

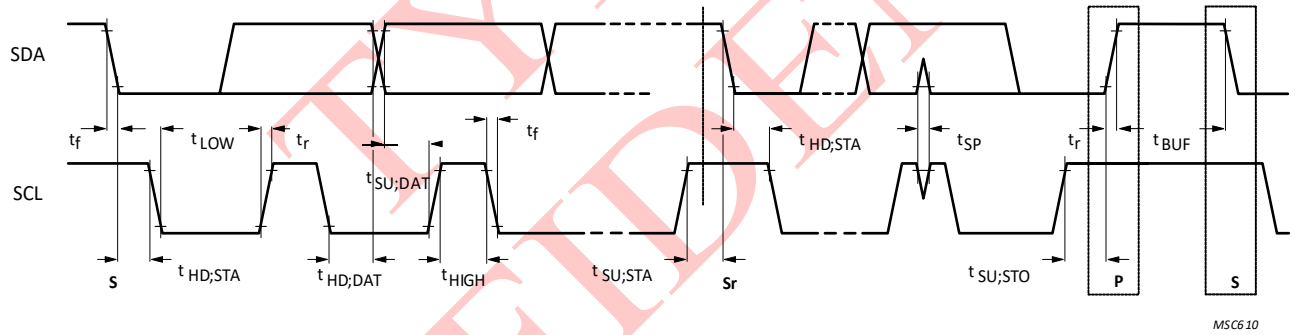


Figure10 I²C Timing

Table3 I²C Timing Parameters(1)

PARAMETER	SYMBOL	MIN	MAX	UNIT
SCL clock frequency	f_{SCL}	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	0.6	–	us
LOW period of the SCL clock	t_{LOW}	1.3	–	us
HIGH period of the SCL clock	t_{HIGH}	0.6	–	us
Set-up time for a repeated START condition	$t_{SU;STA}$	0.6	–	us
Data hold time	tHD;DAT	0(2)	–	us
Data set-up time	$t_{SU;DAT}$	100(4)	–	ns
Rise time of both SDA and SCL signals	tr	–	300	ns
Fall time of both SDA and SCL signals	tf	–	300	ns
Set-up time for STOP condition	$t_{SU;STO}$	0.6	–	us
Bus free time between a STOP and START condition	t_{BUF}	1.3	–	us
Capacitive load for each bus line	Cb	–	400	pF

Noise margin at the LOW level for each connected device (including hysteresis)	V_{nL}	$0.1V_{DD}$	–	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{nH}	$0.2V_{DD}$	–	V

Notes

1. All values referred to VIHmin and VILmax levels (see Table2).
2. A device must internally provide a hold time of at least 300ns for the SDA signal(referred to the VIHmin of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement tSU;DAT⩾250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line tr max + tSU;DAT = 1000 + 250 = 1250 ns (according to the Standard-mode I2C-bus specification) before the SCL line is released.

6 Application Information

Typical application for HX32062S is showing below:

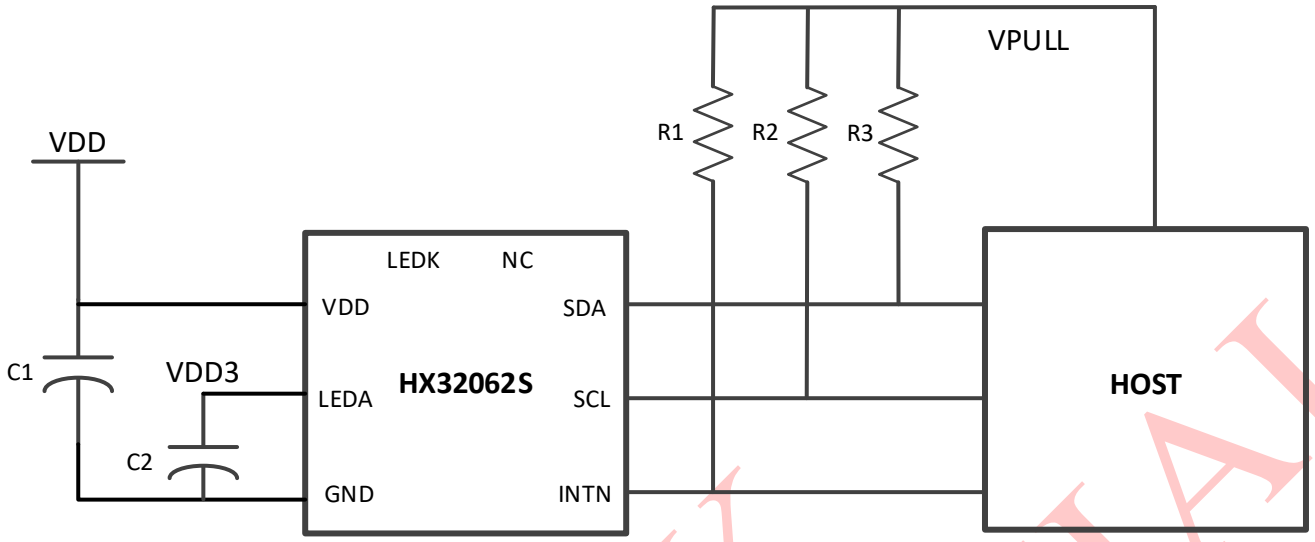


Figure11 Typical Application Schematic

And the device value is listed below:

Table4 I²C Timing Parameters

DEVICE NAME	Value	Description
VDD	1.8V	Low noise
LEDA	2.7~3.6V	Low noise
VPULL	VDD~3.6V	
C1	10uF	
C2	10uF	
R1	2.2k	
R2	2.2k	
R3	2.2k	

7 Package and Reel Information

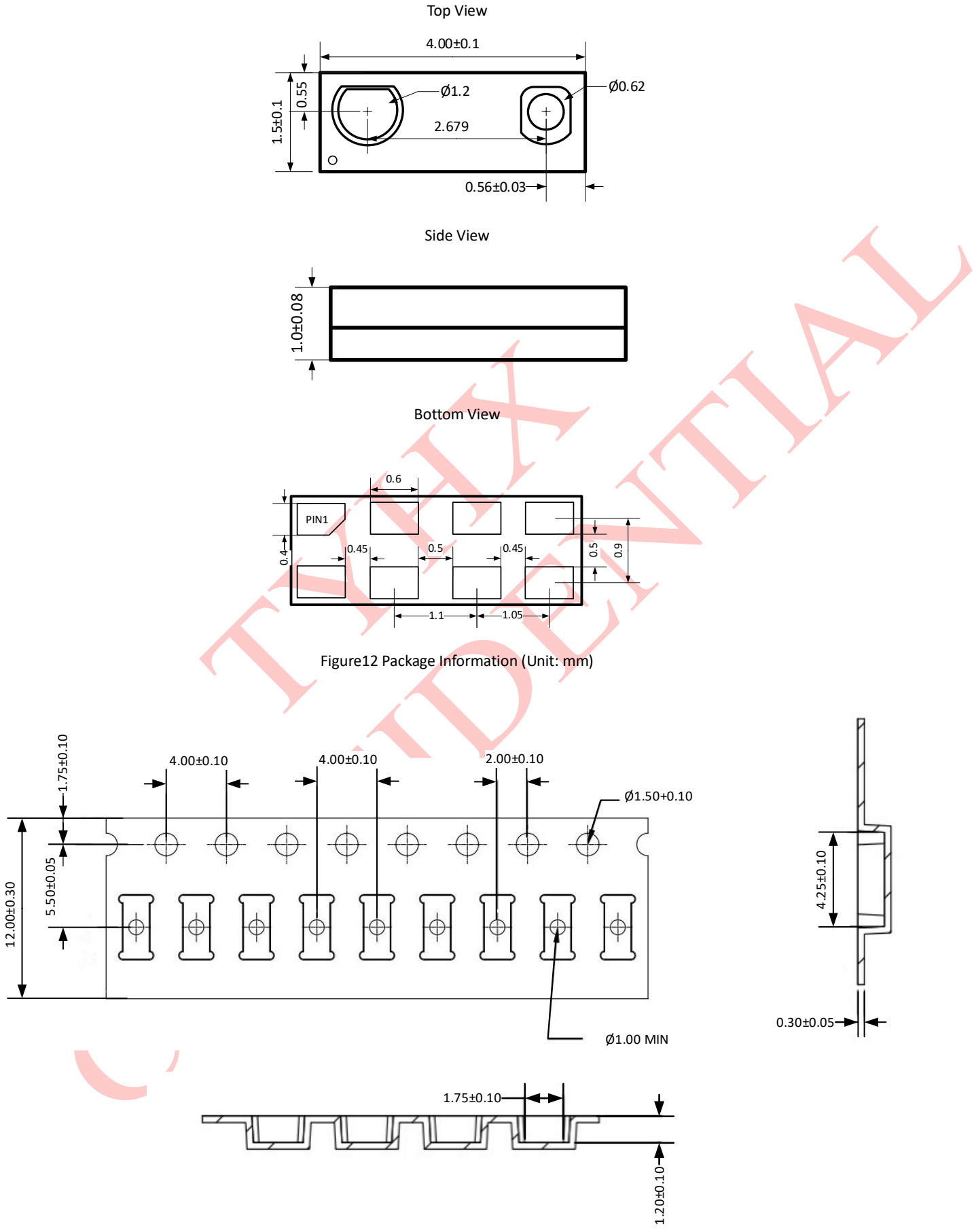
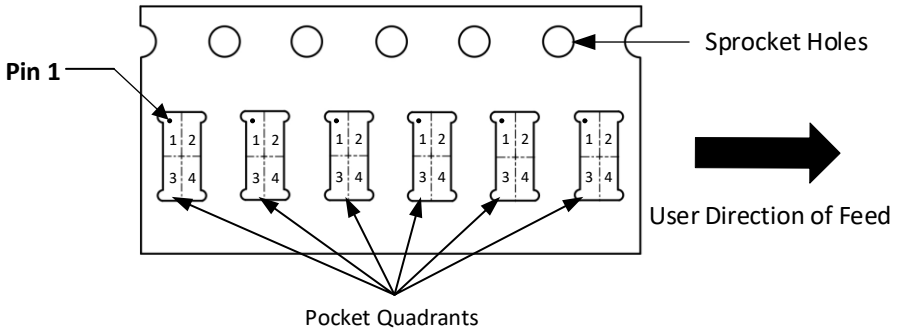
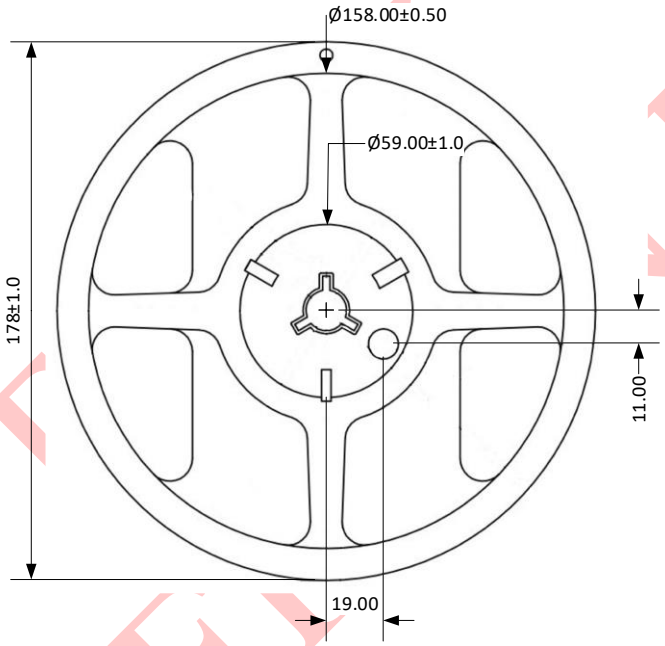


Figure12 Package Information (Unit: mm)

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE





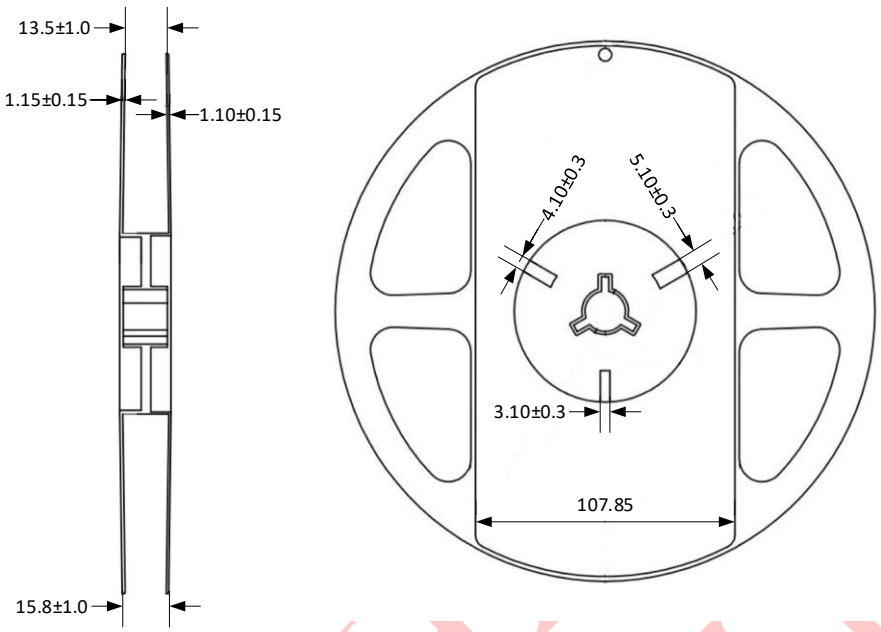


Figure12 Reel Information (Unit: mm)

Notes:

All linear dimensions are in mm. Dimension tolerance is ±0.05mm unless otherwise noted.

8 Soldering Information

The module has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate. The process, equipment, and material used in these tests are detailed below. The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

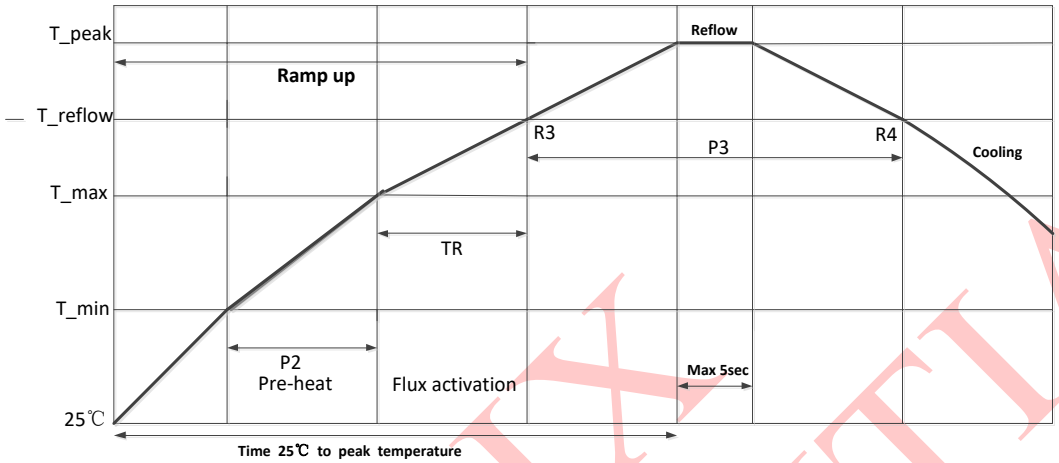


Figure13 Solder reflow profile grape

Table5 Solder Reflow Profile

	Peak temperature (Tpeak)	250-255℃; Max 5sec
Pre-Heat	Temperature min (Tmin)	150℃; 2℃/Sec
	Temperature max(Tmax)	150-217℃； 100S to 180S
	P2：（T min to max）	90-110s
Time maintain above	Temperature (Tre flow)	217℃
	Time (P3)	60-90sec
	R3 Slope (from 217℃ to peak)	2℃/sec(typ) to 2.5℃/sec(max)
	R4 Slope (from peak to 217℃)	1.5℃/sec(typ) to 4℃/sec(max)
	Time to peak temperature	480s Max
	Cooling down slope (peak to 217℃)	2-4℃/sec

REVISION HISTORY

Version	Date	Comment
1.0	Aug 18 2020	Initial version