HX3605 Data Sheet v1.0

Product Definition

HX3605 is an ultra-low power, high performance optical sensor with integrated on-chip photodiode for Wearable, Heart-Rate Monitor and Bio-sensor.

Description

HX3605 is an ultra-low power, high performance optical sensor with I2C interface for Wearable, Heart-Rate Monitor and Bio-sensor. HX3605 integrates a transmitter and a receiver. The receiver has an on-chip photodiode, an offset IDAC and a high-resolution ADC. The transmitter has three LED driver ports sharing a 6bit current driver. Both transmitting and receiving path have very high dynamic range, which is desirable to process small PPG signals.

Features

Accurate, Continuous Heart-Rate Monitoring:

1. Better than 90-dB dynamic range for accurate heart-rate detection
2. Support four phase data in each conversion period
3. Low power for continuous operation on a wearable device : 20 μA for an LED, 27 μA for the Receiver

@ FS=25Hz，LED on time = 32uS , LED driver =25mA

Transmitter:

1. 6-Bit programmable LED current up to 200 mA
2. Programmable LED on time from 8us to 512us
3. Support 3 LEDs for optimized SpO2, HRM, and off-wrist detection
4. Ultra-low current of 20μA is adequate for a typical heart-rate monitoring scenario:

@ FS=25Hz, LED on time = 32uS, LED driver = 25mA

Receiver:

1. 19-Bit representation of the current Input from a photodiode in unipolar straight binary format
2. Individual DC offset subtraction IDAC (Up to ±32μA) at integrator input for each phase
3. Integrator gain adjustment cap. range 4 to 64pf
4. Software sleep mode: less than 0.7 μA current

Pulse Frequency: 1 SPS to 1000 SPS
FIFO With 32-Sample Depth
1.6~3.6V I2C Interface
Operating Temperature Range: -30℃ to 80℃
Supplies:

1. LEDA =3.3~4.6 V
2. VDDA =2.7~3.6 V

Applications

1. **Optical Heart-Rate Monitoring (HRM)**
2. **Heart-Rate Variability (HRV)**
3. **Pulse Oximetry (SpO2) Measurements**
4. **Maximum Oxygen Consumption (VO2 Max)**

Package Information

2.65×2.0×0.7mm, 0.45mm pitch OLGA12

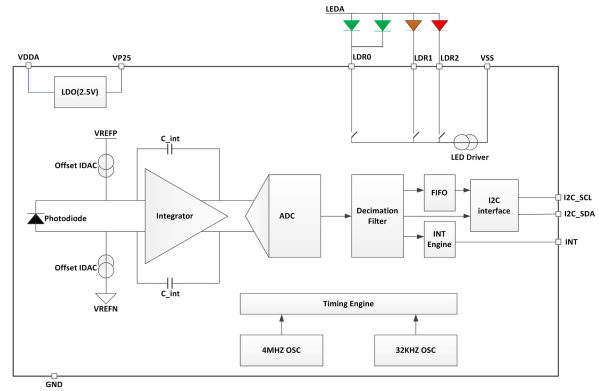

Figure 1. Simplified Block Diagram

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Pin Configuration

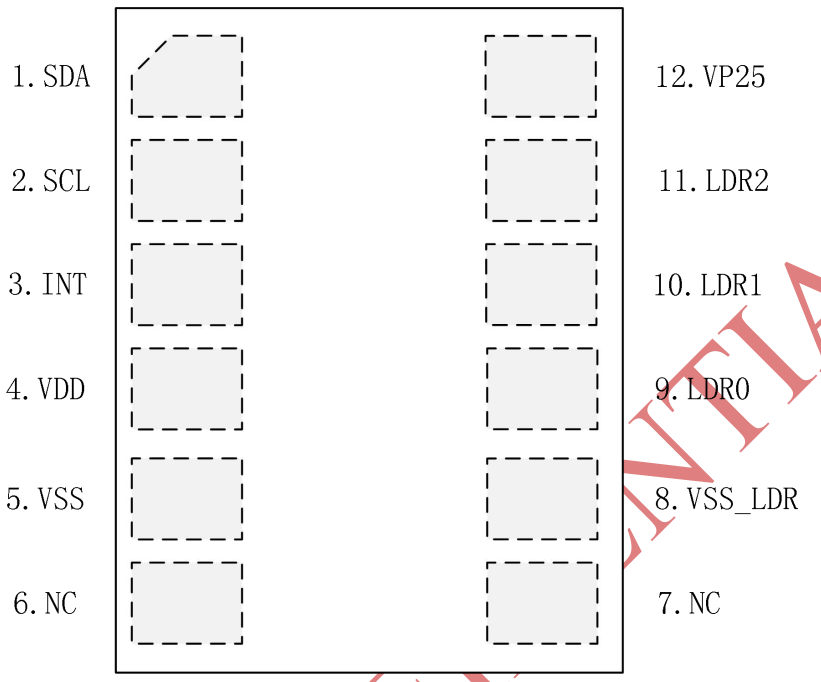


Figure 2. HX3605 Top View Pin Configuration

PIN List

Table 1 HX3605 PIN list

Pin	Name	Type	Description
1	SDA	D	Serial data I/O for I^2C
2	SCL	D	Clock signal for I^2C serial data
3	INT	D	Interrupt output, selectable open drain(default) or cmos
4	VDD	A	Power supply voltage
5	VSS	A	Power supply ground
6	NC		Do not connect, keep floating
7	NC		Do not connect, keep floating
8	VSS_LDR	A	Power supply ground for LED drivers
9	LDR0	A	LED driver0, up to 200mA
10	LDR1	A	LED driver1, up to 200mA
11	LDR2	A	LED driver2, up to 200mA
12	VP25	A	Internal 2.5V LDO output

Specifications

Absolute Maximum Rating(T_a=25℃, unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Supply voltage	-	-	4.0	V
V_{I2c_bus}	II2C Supply voltage	1.6		3.6	V
V_{OUT_MR}	Output voltage [INT]	-0.3		3.6	V
Tstg	Storage temperature	-40	-	85	℃
Tjmax	Maximum Junction Temperature	-	-	125	℃
ESD	ESD tolerance, human body model	±2000			V

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Supply voltage	2.7	3.3	3.6	V
LEDA	Transmit supply voltage	3.3		4.6	V
Ta	Operation temperature, functional	-30	-	80	℃
	Operation temperature, best performance	-20	-	65	℃
VIN	Input voltage [SCL SDA]	1.7	3.3	3.6	V
FI2C	Clock frequency of I2C	-	-	400	KHz

Electrical Characteristics

Minimum and maximum specifications are at temperature = –30°C to 80°C, typical specifications are at 25°C. VDD= V_{I2c_bus} =3.3V, LEDA= 4V, 25Hz date output rate, LED driver current 25mA, led on time= 32uS, 32KHz and 4MHz internal clock, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PULSE REPETITION FREQUENCY					
PRF		1		1000	SPS
RECEIVER					
Offset cancellation DAC current range	10-bit IDAC	- 32		32	uA
Offset cancellation DAC current step		31.25			nA
Integrator gain setting (Cint)	4 bit control	4		64	pF
Integrator capacitor step		4			pF
TRANSMITTER					
LED current range	6 bit control	0		200	mA
LED on time	8 bit control	0		510	uS
CLK (Internal 4MHz Oscillator , used to generate ADC timing)					
Frequency		4			MHz
Accuracy	Room temperature	±1%			
CLK (Internal 32KHz Oscillator , used to generate PRF and INT timing)					
Frequency		32			KHz
Accuracy	Room temperature	±1%			
I2C INTERFACE					
Maximum clock speed		800			KHz
I2C slave address		0x44(7bit)			HEX
PERFORMANCE					
Receiver DR(dynamic range)		91			dB
Transmitter DR(dynamic range)		90			dB
Number of average	Within each PRF cycle	1		32	
CURRENT CONSUMPTION					
Receiver current	Data conversion state	< 750			uA
	PRF wait state	< 4			uA

	Solftware sleep state	< 1			uA
TX LED current	Normal operation	20			uA
	Solftware turnoff mode	< 0.1			uA
DIGITAL INPUTS					
High-level input voltage		0.8* V_{I2c_bus}		V_{I2c_bus}	V
Low-level input voltage		0		0.2* V_{I2c_bus}	V
DIGITAL OUTPUTS					
High-level output voltage		V_{I2c_bus}			V
Low-level output voltage		0			V

(1)PRF refers to the rate at which samples from each of the two phases are output from the sensor.

Detailed Description

Overview

HX3605 internally integrates photodiode, transmitter and receiver for optical heart rate monitoring and pulse oxygen saturation measurement applications. The system is characterized by a parameter called pulse repetition frequency (PRF), which determines the repetition period of the operation sequence. Each cycle of PRF generates four 19 bit digital samples at the output of AFE, and each sample is stored in a separate register.

Functional Block Diagram

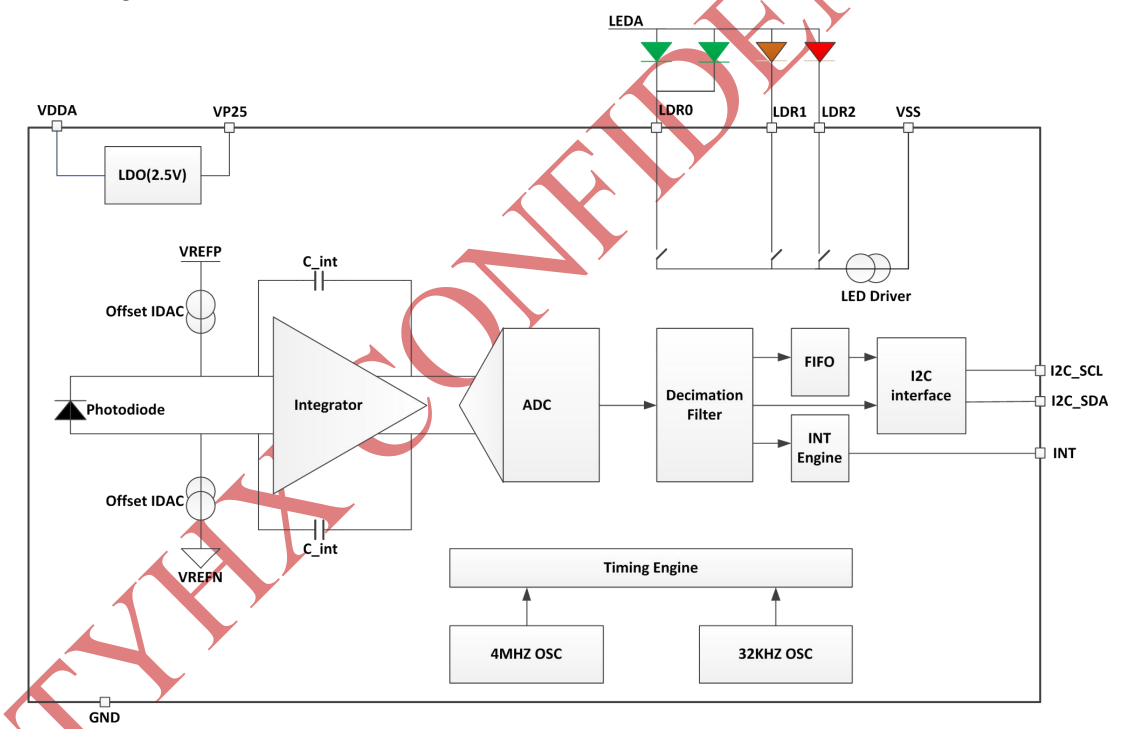


Figure 3. Functional Block Diagram

Digital State Machine Diagram

State machine is a synchronous interface for interactive data between digital and analog. PRF is determined by 32K CLK, and all timings are connected with CLK_ 4m synchronous, completing four functions: sleep, idle and PS0_ PS (output data ps0_data1), PS0_ ALS (output data ps0_data2), PS1_ PS (output data ps1_data1), PS1_ ALS (output data ps1_data2).

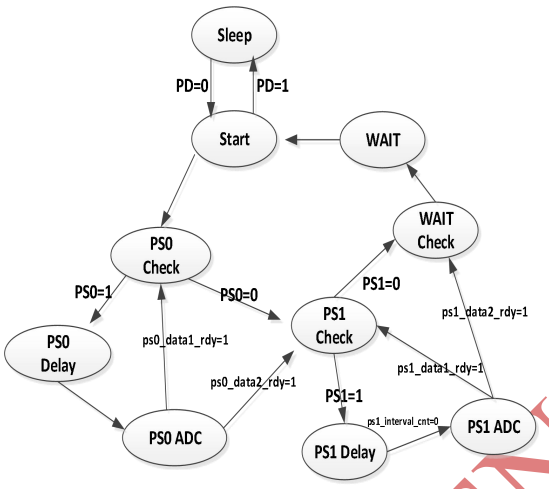


Figure 4. Chip State Machine Diagram

Integrator

The receiving part contains a photodiode. The signal current from the photodiode is converted into a differential voltage through an integrator. The integrator gain is set by its integrating capacitor (Cint) and can be programmed from 4pF to 64pF through register 0x23. The DC offset IDAC current is used to cancel the DC part of the signal. The signal chain remains fully differential throughout the receiver channel so that common mode noise and noise on the power supply can be well suppressed.

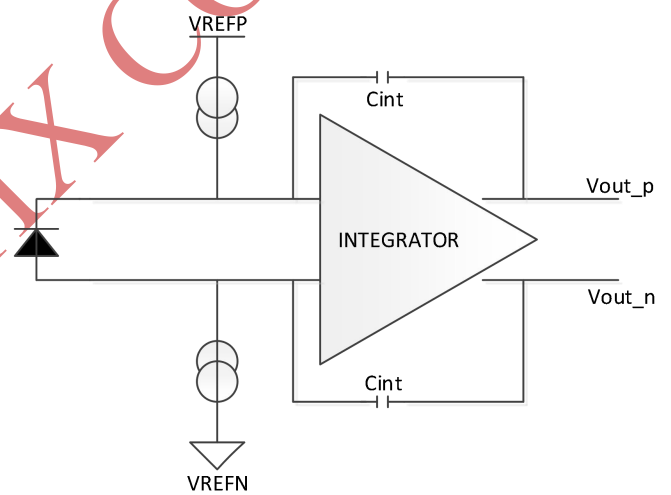


Figure 5. PPG Signal Input Circuit

Integrator MODE: VOUT = Vout_P – Vout_N = 2×(I_signal – I_offset) ×T_int×Cint;

Offset IDAC

A typical optical heart-rate signal has a DC component and an AC component. Higher integrator gain can maximize the output AC signal. In order to eliminate the influence of DC level on the allowable AC signal gain, a current digital to analog converter (IDAC) is placed at the input of the device. By setting the programmable cancellation current (based on the DC current signal level), the effective signal obtained by the integrator can be reduced significantly. In each of the four phases of operation, the cancellation current is automatically presented to the input of the integrator. The ability to set different cancellation current in each of the four phases can be used to eliminate the ambient current in the ambient phase. During the LED on phase, this function can be used to offset the sum of ambient current and DC current of heart rate signal.

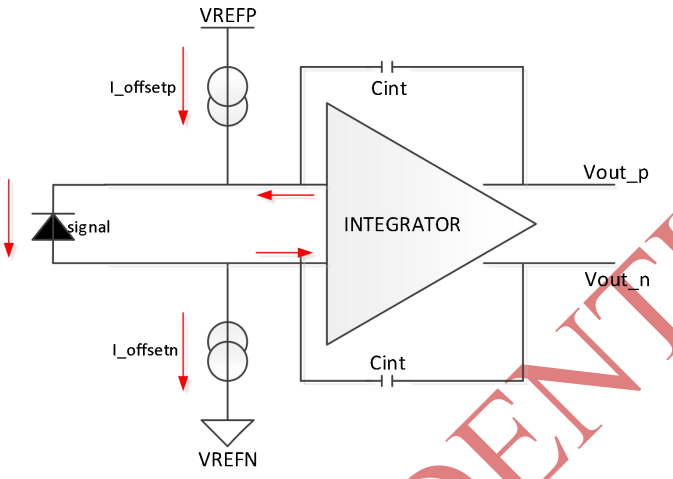


Figure 6. Offset IDAC

LED Driver

The device has an internal current DAC for output current control. PS0 phase led driver controls output current through register 0x21 < bit5: bit0 >. PS1 phase led driver controls the output current through register 0x22 < bit5: bit0 >.

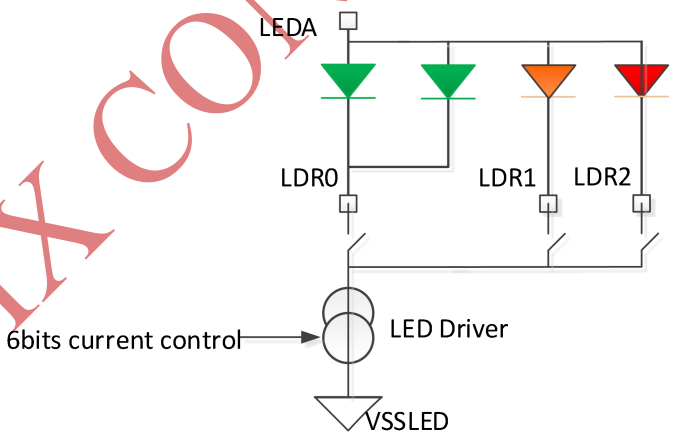


Figure 7. LED Driver Circuit

Analog-to-Digital Converter (ADC)

The hx3605 has a two-stage one bit sigma delta ADC that provides a maximum 19 bit representation of the current from the photodiode. ADC has configurable over sampling rate (OSR) through register 0x10 < bit3: bit0 >. ADC code corresponding to various sampling phases can be read from 24 bit registers (0xa0 ~ 0xab) in unipolar direct binary format. The ADC full-scale input range is ± 2.5 V, spanning bit18 to bit0. The mapping from ADC input voltage to ADC code is shown in table below (ADC over sampling rate = 1024)

DIFFERENTIAL INPUT VOLTAGE AT ADC INPUT(Vout_p –Vout_n)	24-BIT ADC OUTPUT CODE (Binary)	20-BIT ADC OUTPUT CODE (Decimalism)
- 2.5V	0000 0000 0000 0000 0000	0
0	0100 0000 0000 0000 0000	262144
+2.5V	0111 1111 1110 1111 1110	524030

ADC over sample rate = 512

DIFFERENTIAL INPUT VOLTAGE AT ADC INPUT(Vout_p –Vout_n)	24-BIT ADC OUTPUT CODE (Binary)	20-BIT ADC OUTPUT CODE (Decimalism)
- 2.5V	0000 0000 0000 0000 0000	0
0	0000 1111 1110 0000 0001	65025
+2.5V	0010 0000 0000 1011 1011	131259

ADC over sample rate = 256

DIFFERENTIAL INPUT VOLTAGE AT ADC INPUT(Vout_p –Vout_n)	24-BIT ADC OUTPUT CODE (Binary)	20-BIT ADC OUTPUT CODE (Decimalism)
- 2.5V	0000 0000 0000 0000 0000	0
0	0000 0011 1111 1000 0000	16256
+2.5V	0000 1000 0000 1000 0000	32896

ADC over sample rate = 128

DIFFERENTIAL INPUT VOLTAGE AT ADC INPUT(Vout_p –Vout_n)	24-BIT ADC OUTPUT CODE (Binary)	20-BIT ADC OUTPUT CODE (Decimalism)
- 2.5V	0000 0000 0000 0000 0000	0
0	0000 0000 1111 1100 0000	4032
+2.5V	0000 0010 0000 0100 0000	8256

Digital Interface

I2C Data format

The I2C bus protocol was developed by Philips (now NXP). The device supports the standard writing and reading protocol. The 7-bit device address is 0x44. The register index will automatically increase by 1 after the addressed register has been accessed (read or write).And the format is shown as following:

A Acknowledge (0)

P Stop Condition

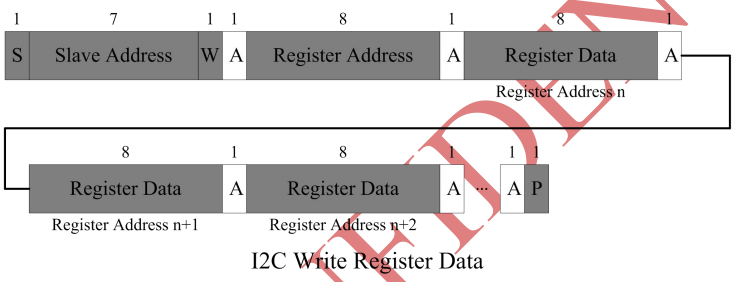
R Read (1)

S Start Condition

W Write (0)

Sr Repeated Start Condition

■ Master-to- Slave
□ Slave-to-Master



I2C Write Register Data

I2C Read Register Data

Figure 8. I2C Data Format Diagram

I2C Electrical Characteristics

Table 2 Electrical Characteristics

PARAMETER	SYMBOL	STANDARD-MODE		FAST-MODE		UNIT
		MIN	MAX	MIN	MAX	
LOW level input voltage: fixed input levels (V_{I2c_bus} =1.8V)	VIL	0.5	0.54	n/a	n/a	V
			0.3 V_{I2c_bus}	0.5	0.3 V_{I2c_bus}	
HIGH level input voltage: fixed input levels (V_{I2c_bus} =1.8V)	VIH	1.26	n/a	1.26	n/a	V
		0.7 V_{I2c_bus}	Note(2)	0.7 V_{I2c_bus}	Note(2)	
Hysteresis of Schmitt trigger inputs: V_{I2c_bus} > 2 V V_{I2c_bus} < 2 V	Vhys	n/a	n/a	0.05Vbus	–	V
		n/a	n/a	0.1Vbus	–	
LOW level output voltage (open drain or open collector) at 3 mA sink current: V_{I2c_bus} > 2 V V_{I2c_bus} < 2 V	VOL1	0	0.4	0	0.4	V
	VOL2	n/a	n/a	0	0.2 V_{I2c_bus}	
Output fall time from VIHmin to VILmax with a bus capacitance from 10 pF to 400 pF	tof	–	250(4)	20+0.1 Cb(3)	250(4)	ns
Pulse width of spikes which must be suppressed by the input filter	tSP	n/a	n/a	0	50	ns
Input current each I/O pin with an input voltage between 0.1VDD and 0.9VDDmax	Ii	-10	10	-10(5)	10(5)	A
Capacitance for each I/O pin	Ci	-	10	-	10	pF

Notes

1.Devices that use non-standard supply voltage switch don't conform to the intended I2C-bus system levels must relate input levels to the VDD voltage to which the pull-up resistors Rp are connected.

2.Maximum $V_{IH} = V_{DDmax}$ + 0.5V.

3.C_b = capacitance of one bus line in pF.

4.The maximum t_f for the SDA and SCL bus lines quoted in Table(300ns) is longer than the specified maximum t_{of} for the output stages (250 ns). This allows series protection resistors (R_S) to be connected between the SDA/SCL pins and the SDA/SCL bus lines without exceeding the maximum specified tf.

5.I/O pins of Fast-mode devices must not obstruct the SDA and SCL lines if VDD is switched off.

n/a = not applicable

I2C Timing

The I2C Timing is as following figure:

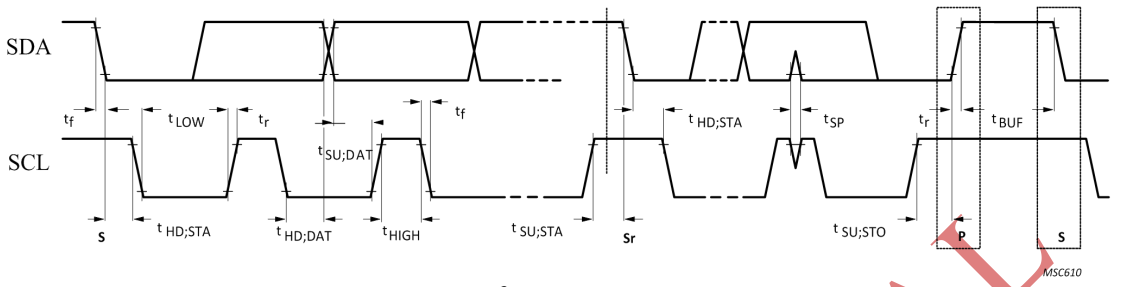


Figure 9. I²C Timing

Table 3 I²C Timing Parameters(1)

PARAMETER	SYMBOL	STANDARD-MODE		FAST-MODE		UNIT
		MIN	MAX	MIN	MAX	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	4.0	–	0.6	–	us
LOW period of the SCL clock	t_{LOW}	4.7	–	1.3	–	us
HIGH period of the SCL clock	t_{HIGH}	4.0	–	0.6	–	us
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	–	0.6	–	us
Data hold time	$t_{HD;DAT}$	0(2)	3.45(3)	0(2)	0.9(3)	us
Data set-up time	$t_{SU;DAT}$	250	–	100(4)	–	ns
Rise time of both SDA and SCL signals	tr	–	1000	20+0.1Cb(5)	300	ns
Fall time of both SDA and SCL signals	tf	–	300	20+0.1Cb(5)	300	ns
Set-up time for STOP condition	$t_{SU;STO}$	4.0	–	0.6	–	us
Bus free time between a STOP and START condition	t_{BUF}	4.7	–	1.3	–	us
Capacitive load for each bus line	Cb	–	400	–	400	pF

Notes

1.All values referred to V_{IHmin} and V_{ILmax} levels (see Table2).

2.A device must internally provide a hold time of at least 300ns for the SDA signal(referred to the VIHmin of the SCL signal) to bridge the undefined region of the falling edge of SCL.

3.The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

4.A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement tSU;DAT≥250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line tr max + tSU;DAT = 1000 + 250 = 1250 ns (according to the Standard-mode I2C-bus specification) before the SCL line is released.

5.Cb=total capacitance of one bus line in pF. If mixed with Hs-mode devices, faster fall-times according to Table2 are allowed.

Note： n/a = not applicable

Registers

Registers List

Address	Name	R/W	Function	Default
0x00	ID	RO	RA_PART_ID	0x25
0x01	POWER DOWN	RO	POWER DOWN[0]	0x0C
0x02	PS0_DATA1_OUT	RO	PS0_DATA1_OUT[7:0]	0x00
0x03		RO	PS0_DATA1_OUT[15:8]	0x00
0x04		RO	PS0_DATA1_OUT[19:16]	0x00
0x05	PS0_DATA2_OUT	RO	PS0_DATA2_OUT[7:0]	0x00
0x06		RO	PS0_DATA2_OUT[15:8]	0x00
0x07		RO	PS0_DATA2_OUT[19:16]	0x00
0x08	PS1_DATA1_OUT	RO	PS1_DATA1_OUT[7:0]	0x00
0x09		RO	PS1_DATA1_OUT[15:8]	0x00
0x0A		RO	PS1_DATA1_OUT[19:16]	0x00
0x0B	PS1_DATA2_OUT	RO	PS1_DATA2_OUT[7:0]	0x00
0x0C		RO	PS1_DATA2_OUT[15:8]	0x00
0x0D		RO	PS1_DATA2_OUT[19:16]	0x00
0x10	PS0/1_EN	RW	PS0/1 ENALE AND ADC OSR SELECT	0x00
0x11	PRF_CFG	RW	PRF_CYCLE_I2C[7:0]	0x00
0x12		RW	PRF_CYCLE_I2C[11:8]	0x03
0x13	PS1_PRF_ INTERVAL	RW	PS1 INTERVAL NUMBER	0x00
0x15	LED_EN_NUM	RW	LED_EN SIGNAL LENGTH	0x00
0x16	PS_CP_AVG_NUM_SEL	RW	PS0/1 IN PRF AVERAGE	0x00
0x17	PS_AVG_NUM_SEL	RW	PS0/1 AVERAGE DATA NUMBER CONFIGURATION	0x00
0x18	DCCANCEL_PS0_ DATA1	RW	DCCANCEL_PS0_DATA1_I2C[7:0]	0x00
0x19		RW	DCCANCEL_PS0_DATA1_I2C[9:8]	0x03
0x1A	DCCANCEL_PS0_ DATA2	RW	DCCANCEL_PS0_DATA2_I2C[7:0]	0x00
0x1B		RW	DCCANCEL_PS0_DATA2_I2C[9:8]	0x00
0x1C	DCCANCEL_PS1_ DATA1	RW	DCCANCEL_PS1_DATA1_I2C[7:0]	0x00
0x1D		RW	DCCANCEL_PS1_DATA1_I2C[9:8]	0x00
0x1E	DCCANCEL_PS1_ DATA2	RW	DCCANCEL_PS1_DATA2_I2C[7:0]	0x00
0x1F		RW	DCCANCEL_PS1_DATA2_I2C[9:8]	0x00
0x20	PS0_ COMPONENTS _SEL	RW	PS0 IR_PDEN SEL[7]	0x00
			PS0 EXT_PDEN SEL[6]	
			PS0 LED CURRENT CONFIGURATION [5:0]	
0x21	PS1_ COMPONENTS _SEL	RW	PS1 IR_PDEN SEL[7]	0x00
			PS1 EXT_PDEN SEL[6]	
			PS1 LED CURRENT CONFIGURATION [5:0]	
0x22	PS_LDR_SEL	RW	PS0/1 LED DRIVER SELECT	0x00
0x23	PS_INTCAP_SEL	RW	PS0/1 INTCAP VALUE SELECT	0x00
0x26	THRES_INT_EN	RW	THRESHOLD INTERRUP ENABLE	0x0F
0x27	INT_EN_CFG	RW	FIFO ALMOST FULL AND PRF INTERRUPT ENABLE	0x00
0x28	THRES_CNT_NUM_SEL	RW	NUMBER OF OVER THRESHOLD TRIGGER INTERRUPS SELECT	0x00
0x29	THRES_VALUE	RW	THRES_VALUE [7:0]	0xFF
0x2A		RW	THRES_VALUE [15:8]	0x7F
0x2B	INT_CFG	RW	INCLUDING INTERRUPT OUTPUT POLARITY AND PIN MODE SELECT	0x1C
0x2C	INT_WIDTH_I2C	RW	INT MINIMUM PULSE WIDTH	0x1F
0x2D	FIFO_CFG1	RW	FIFO CONFIGURATION RELATED	0x00
0x2E	FIFO_CFG2	RW	FIFO CONFIGURATION RELATED	0x10
0x2F	FIFO_CFG3	RO	FIFO CONFIGURATION RELATED	0x00
0x30	FIFO_CFG4	RO	FIFO CONFIGURATION RELATED	0x00
0x31	FIFO_DATA OUT	RO	FIFO_DATAOUT[7:0]	0x00

0x32		RO	FIFO_DATAOUT[15:8]	0x00
0x33	FIFO_DATA OUT	RO	FIFO_DATAOUT[22:16]	0x00

Register Description

Register(0x00)

Address	Type	Default	Name	BIT	Default	Description
0x00	RO	0x25	Device_ID	7:0	25	HX3605 chip ID

Register(0x01)

Address	Type	Default	Name	BIT	Default	Description
0x01	RW	0x0C	Int_core	3	1	Int_core
			Standby	2	1	Standby
			PDon_reset_out	1	0	PDon_reset_out
			Power down	0	0	1 : Power down 0 : Power on

Register(0x02,0x03,0x04)

Address	Type	Default	Name	BIT	Default	Description
0x02	RO	0x00	PS0_data1_out[7:0]	7:0	00	PS0_data1_out
0x03	RO	0x00	PS0_data1_out[15:8]	7:0	00	
0x04	RO	0x00	PS0_data1_out[19:16]	3:0	00	

Register(0x05,0x06,0x07)

Address	Type	Default	Name	BIT	Default	Description
0x05	RO	0x00	PS0_data2_out[7:0]	7:0	00	PS0_data2_out
0x06	RO	0x00	PS0_data2_out[15:8]	7:0	00	
0x07	RO	0x00	PS0_data2_out[19:16]	3:0	00	

Register(0x08,0x09,0x0A)

Address	Type	Default	Name	BIT	Default	Description
0x08	RO	0x00	PS1_data1_out[7:0]	7:0	00	PS1_data1_out
0x09	RO	0x00	PS1_data1_out[15:8]	7:0	00	
0x0A	RO	0x00	PS1_data1_out[19:16]	3:0	00	

Register(0x0B,0x0C,0x0D)

Address	Type	Default	Name	BIT	Default	Description
0x0B	RO	0x00	PS1_data2_out[7:0]	7:0	00	PS1_data2_out
0x0C	RO	0x00	PS1_data2_out[15:8]	7:0	00	
0x0D	RO	0x00	PS1_data2_out[19:16]	3:0	0	

Register(0x10)

Address	Type	Default	Name	BIT	Default	Description
0x10	RW	0x00	PS1_en_i2c	5	0	PS1 enable
			PS0_en_i2c	4	0	PS0 enable
			PS1_valid_data_cycle_sel_i2c	3:2	0	PS1 ADC over sampling rate: 0x0 128 0x1 256 0x2 512 0x3 1024
			PS0_valid_data_cycle_sel_i2c	1:0	0	PS0 ADC over sampling rate: 0x0 128 0x1 256 0x2 512 0x3 1024

Register(0x11,0x12)

Address	Type	Default	Name	BIT	Default	Description
0x11	RW	0x00	PRF_cycle_i2c[7:0]	7:0	0	PRF configuration
0x12	RW	0x03	PRF_cycle_i2c[11:8]	3:0	3	

Register(0x13)

Address	Type	Default	Name	BIT	Default	Description
0x13	RW	0x00	PS1_interval_i2c	7:0	0	PS1 Interval number

Register(0x15)

Address	Type	Default	Name	BIT	Default	Description
0x15	RW	0x00	Led_en_num	7:0	0	Led_en signal length =led_en_num*8

Register(0x16)

Address	Type	Default	Name	BIT	Default	Description
0x16	RW	0x00	PS1_cp_avg_num_sel	6:4	000	PS1 In-PRF average number: 0x0: 1 0x1: 4 0x2: 8 0x3: 16 0x4: 32
			PS0_cp_avg_num_sel	3:0	0	PS0 In-PRF average number: 0x0: 1 0x1: 4 0x2: 8 0x3: 16 0x4: 32

Register(0x17)

Address	Type	Default	Name	BIT	Default	Description
0x17	RW	0x00	PS1_avg_num_sel_i2c	3:2	0	PS1 data average number: 0x0 1 0x1 2 0x2 4 0x3 8
			PS0_avg_num_sel_i2c	1:0	0	PS0 data average number: 0x0 1 0x1 2 0x2 4 0x3 8

Register(0x18,0x19)

Address	Type	Default	Name	BIT	Default	Description
0x18	RW	0x00	Dccancel_ps0_data1_i2c[7:0]	7:0	00	PS0_data1 DCCANCEL value
0x19	RW	0x00	Dccancel_ps0_data1_i2c[9:8]	1:0	0	

Register(0x1A,0x1B)

Address	Type	Default	Name	BIT	Default	Description
0x1A	RW	0x00	dccancel_ps0_data2_i2c[7:0]	7:0	00	PS0_data2 DCCANCEL value
0x1B	RW	0x00	dccancel_ps0_data2_i2c[9:8]	1:0	0	

Register(0x1C,0x1D)

Address	Type	Default	Name	BIT	Default	Description
0x1C	RW	0x00	Dccancel_ps1_data1_i2c[7:0]	7:0	00	PS1_data1 DCCANCEL value
0x1D	RW	0x00	Dccancel_ps1_data1_i2c[9:8]	1:0	0	

Register(0x1E,0x1F)

Address	Type	Default	Name	BIT	Default	Description

0x1E	RW	0x00	Dccancel_ps1_data2_i2c[7:0]	7:0	00	PS1_data2 DCCANCEL value
0x1F	RW	0x03	Dccancel_ps1_data2_i2c[9:8]	1:0	0	

Register(0x20)

Address	Type	Default	Name	BIT	Default	Description
0x20	RW	0x00	Ir_pden_ps0_i2c	7	0	PS0 ir_pden sel
			Ext_pden_ps0_i2c	6	0	PS0 ext_pden sel
			PDdrive_ps0_i2c	5:0	0	PS0 led current configuration

Register(0x21)

Address	Type	Default	Name	BIT	Default	Description
0x21	RW	0x00	Ir_pden_ps1_i2c	7	0	PS1 ir_pden sel
			Ext_pden_ps1_i2c	6	0	PS1 ext_pden sel
			PDdrive_ps1_i2c	5:0	0	PS1 led current configuration

Register(0x22)

Address	Type	Default	Name	BIT	Default	Description
0x22	RW	0x00	Ldrsel_ps1_i2c	6:4	0	PS1 led driver select
			Ldrsel_ps0_i2c	2:0	0	PS0 led driver select

Register(0x23)

Address	Type	Default	Name	BIT	Default	Description
0x23	RW	0x00	Intcapsel_ps1_i2c	7:4	0	PS1 int-cap value select
			Intcapsel_ps0_i2c	3:0	0	PS0 int-cap value select

Register(0x26)

Address	Type	Default	Name	BIT	Default	Description
0x26	RW	0x0F	Thres_int_en	4	0	Threshold-interrupt enable
			Data_rdy_int_en	3:0	F	Data ready interrupt enable. Each bit for one phase: [3]:PS1_data2 [2]:PS1_data1 [1]:PS0_data2 [0]:PS0_data1

Register(0x27)

Address	Type	Default	Name	BIT	Default	Description
0x27	RW	0x00	W_almost_full_int_en_i2c	4	0	FIFO almost full interrupt enable
			PRF_cnt_over_strobe_int_en_i2c	0	0	PRF interrupt enable

Register(0x28)

Address	Type	Default	Name	BIT	Default	Description
0x28	RW	0x00	Thres_int_mode	2	0	0：Self clearing interrupt; 1：Interrupt pin output thres_hig_n_low signal;
			Thres_cnt_num_sel	1:0	0	Number of over threshold trigger interrups select： 0: 1 1: 2 2: 4 3: 8

Register(0x29,0x2A)

Address	Type	Default	Name	BIT	Default	Description
0x29	RW	0xFF	thres_level[7:0]	7:0	FF	Thres_value: threshold: thres_level+512 Low-threshold：thres_level-512
0x2A	RW	0x7F	thres_level[15:8]	7:0	7F	

Register(0x2B)

Address	Type	Default	Name	BIT	Default	Description
0x2B	RW	0x1C	Int_polar	4	0	Interrupt output polarity: 0: High Level on 1: Low Level on
			Other_int_pad_en	3	1	Threshold、almost_full、PRF interrupt output to interrupt pin enable
			Data_rdy_int_pad_en	2	1	Data ready Interrupt output to interrupt pin enable
			Int_clr_mode	1:0	0	Interrupt pin mode: 0: Edge pulse mode 1: Level mode

Register(0x2C)

Address	Type	Default	Name	BIT	Default	Description
0x2C	RW	0x1F	Int_width_i2c	6:0	1F	Int minimum pulse width

Register(0x2D)

Address	Type	Default	Name	BIT	Default	Description
0x2D	RW	0x00	FIFO_en	7	0	FIFO enable
			Mult_fifo_int_mode	4	0	0: FIFO only generates one interrupt when it exceeds watermark 1: After FIFO exceeds watermark, a new interrupt will be generated every time a new data is written
			FIFO_data_sel_i2c	3:0	0	0x0: ps0_data1 ,ps0_data2 ps1_data1, ps1_data2 0x1: ps0_data1, ps0_data2 0x2: ps1_data1, ps1_data2 0x3: ps0_data1-ps0_data2 ps1_data1-ps1_data2 0x4: ps0_data1-ps0_data2

Register(0x2E)

Address	Type	Default	Name	BIT	Default	Description
0x2E	RW	0x10	FIFO_watermark_i2c	5:0	10	Set the number for FIFO almost full interrupt

Register(0x2F)

Address	Type	Default	Name	BIT	Default	Description
0x2F	RO	0x00	W_usedword	5:0	0	W_usedword

Register(0x30)

Address	Type	Default	Name	BIT	Default	Description
0x30	RO	0x00	R_usedword	5:0	0	R_usedword

Register(0x31)

Address	Type	Default	Name	BIT	Default	Description
0x31	RO	0x00	FIFO_dataout[7:0]	7:0	0	FIFO_dataout[7:0]

Register(0x32)

Address	Type	Default	Name	BIT	Default	Description
0x32	RO	0x00	FIFO_dataout[15:8]	7:0	0	FIFO_dataout[15:8]

Register(0x33)

Address	Type	Default	Name	BIT	Default	Description
0x33	RO	0x00	Underflow	7	0	Underflow
			FIFO_dataout[22:16]	6:0	0	FIFO_dataout[22:16]

Application Information

Reference Schematic

A typical I2C interface application schematic diagram for HX3605 is shown in Figure 10. The I2C signals and the Interrupt are open-drain outputs and require pull-up resistors (Rp). It is recommended to use 10kΩ resistors when running at 400kbps.

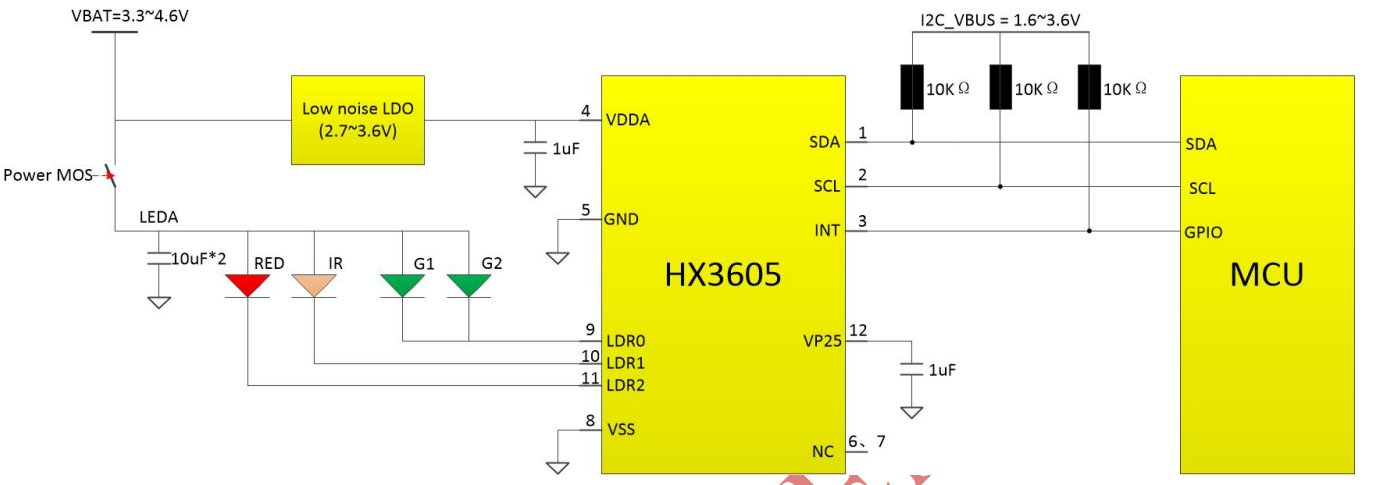
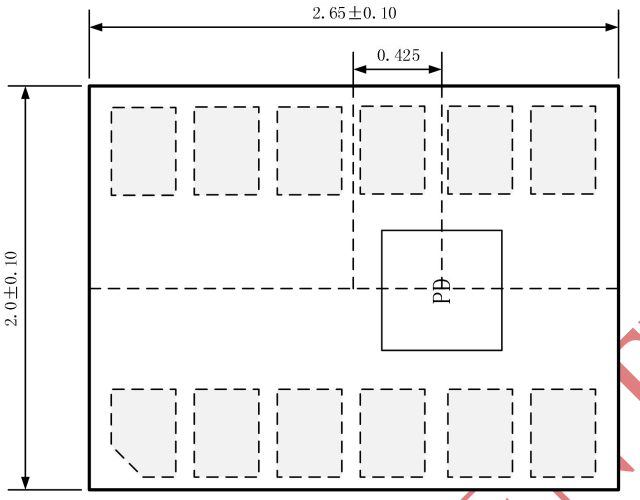


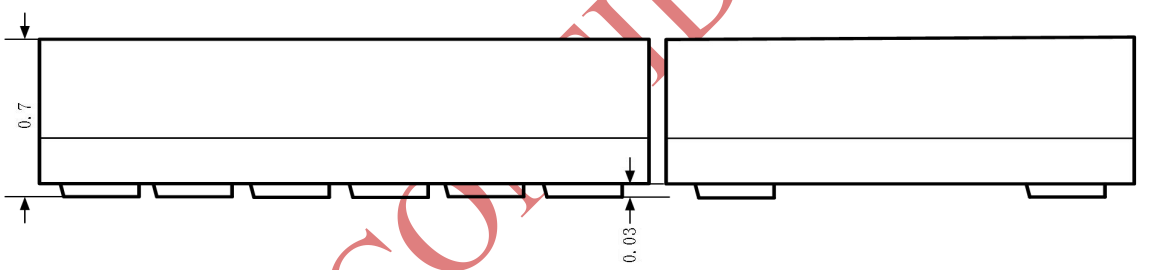
Figure 10. Typical I2C Interface Application Schematic Diagram

Package information

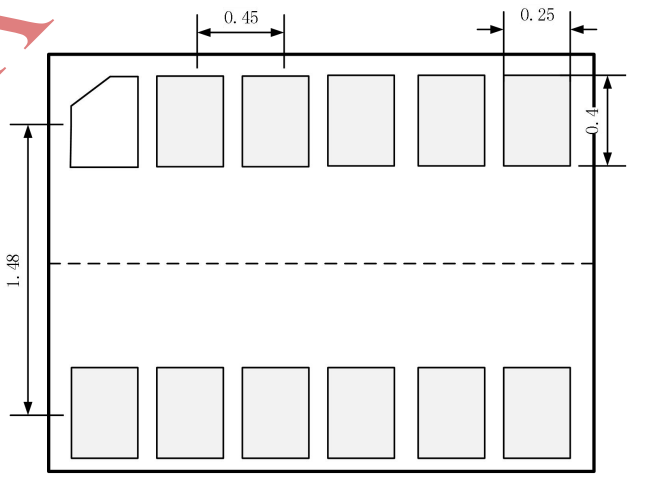
Top View



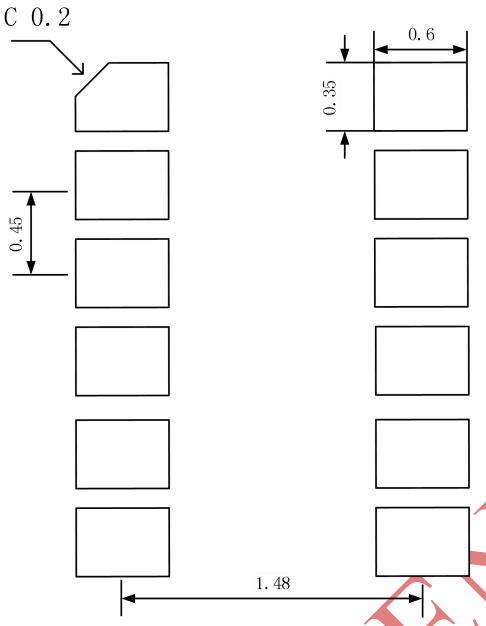
Side View



Bottom View



Recommended PCB Pad Layout



Notes: All linear dimensions are in mm. Dimension tolerance is ±0.05mm unless otherwise noted.

Soldering Information

HX3605 has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate. The process, equipment and materials used in these test are detailed below. The reflow soldering profile describes the expect maximum heat exposure of components during the reflow soldering process. Temperature is measured on top of components. The soldering process should be limited to a maximum of three phases according to this reflow soldering profile.

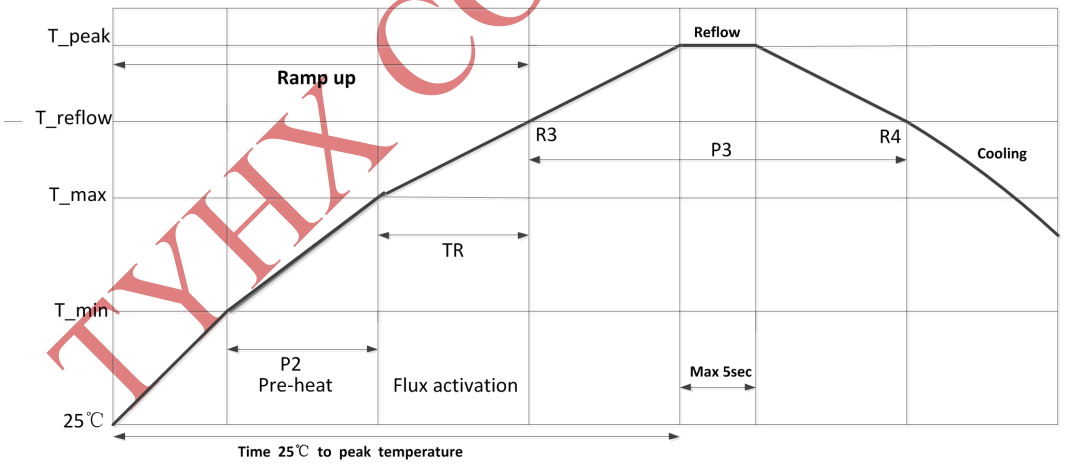


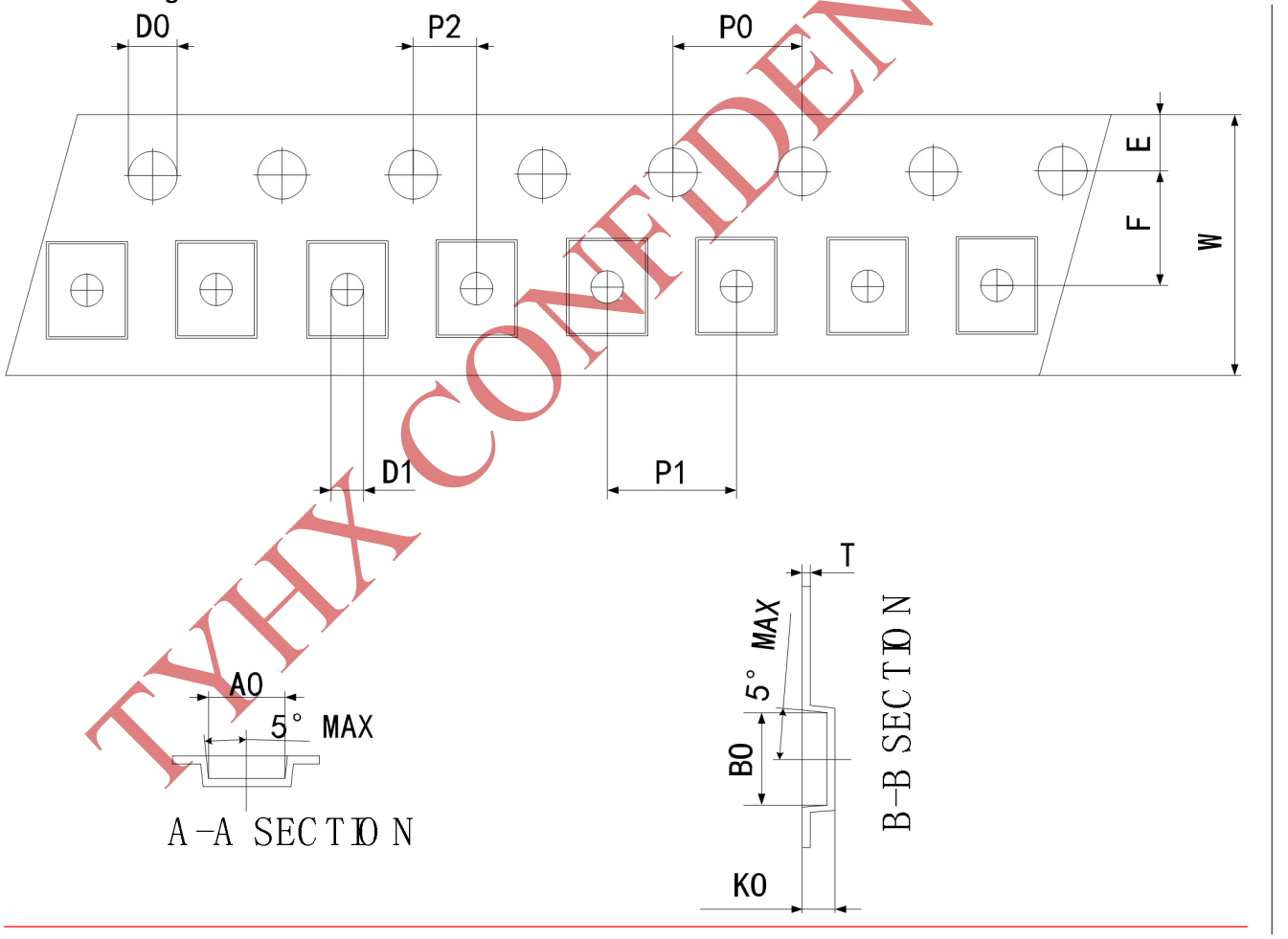
Figure11. HX3605 Reflow Profile Graph

The detail parameters are listed in the following table:

Table 4 Reflow Soldering Profile Parameters

	Peak temperature (Tpeak)	250℃; Max 5sec
Pre-Heat	Temperature min (Tmin)	150℃; 2℃/Sec
	Temperature max(Tmax)	150-217℃ ; 100S to 180S
	P2 ： (T min to max)	90-110s
Time maintain above	Temperature (Treflow)	217 ℃
	Time (P3)	60-90sec
	R3 Slope (from 217℃to peak)	2℃/sec(typ) to 2.5℃/sec(max)
	R4 Slope (from peak to 217℃)	1.5℃/sec(typ) to 4℃/sec(max)
	Time to peak temperature	480s Max
	Cooling down slope (peak to 217℃)	2-4℃/sec

Carrier Drawing



Symbol	A0	B0	K0	P0	P1	P2	T
Spec	2.35±0.05	2.85±0.05	0.85±0.05	4.00±0.10	4.00±0.10	2.00±0.05	0.25±0.02
Symbol	E	F	D0	D1	W	10P0	
Spec	1.75±0.10	3.50±0.05	1.50	1.0MIN	8.00	40.0±0.20	

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